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THESIS

DESIGN OF A VLSI CHARGE-COUPLED DEVICE ANALOG DELAY LINE

by

David R. Gedra

March, 1995

Thesis Advisor: Douglas J. Fouts
Second Reader: Jon T. Butler

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Charge-coupled devices (CCDs) are semiconductor devices which can transfer information, represented by a quantity of electrical charge, from one physical location of the semiconductor substrate to another in a controlled manner with the use of properly sequenced clock pulses. These devices can be applied to imaging, signal processing, logic, and digital storage applications.

In this thesis, the design of an electrically-stimulated CCD analog delay line, using the design tools currently available at the Naval Postgraduate School, is reported on. The major issues addressed are the electrode gate structure and composition, charge confinement techniques, and clocking schemes. Additionally, techniques for inputting and detecting charge packets from the CCD register are examined. The Metal Oxide Semiconductor Integration Service (MOSIS) design rules only permit Bulk Channel Charge-Couple Devices (BCCDs) to be laid out, and not Surface Channel Charge-Coupled Devices (SCCDs).

Restricted to a die size of 2.24 mm length, the electrode gates were chosen to be polysilicon-polysilicon 8 μm length with 2 μm overlap and 20 μm width, giving the BCCD 64 stages. An on-chip four-phase clocking circuit with output drivers on each phase provides the control voltage for the gate electrodes. The small width of the BCCD delay line utilizes only a small portion of the available 2.22 mm die width. Therefore, four different BCCDs were designed in the layout. Two of the BCCDs have a p-diffusion stop to contain the charge laterally as it propagates along the channel while two BCCDs do not. Additionally, two of the BCCDs utilize the charge partition input technique with three control gates and two BCCDs use the dynamic current injection with one control gate.

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ANALOG DELAY LINE

by

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Lieutenant, United States Navy
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Submitted in partial fulfillment of the
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I. INTRODUCTION

A. OVERVIEW OF SYSTEM DESIGN

Figure 1 shows a block diagram of the charge-coupled device analog CCD delay line. An electrical input signal is introduced into the CCDs' input structure. Here a charge packet linearly proportional to the input signal voltage is injected into the CCD register. The register consists of 64 stages of four overlapping electrodes, allowing up to 64 packets to be in the register body at one time. Four clocking signals from the clocking circuit and clock buffers operate the register, one clock signal to each electrode of the stage. The clock signals are in successive order and have a one-quarter period overlap to move the charge packet along the register channel. When the charge reaches the end of the CCD register channel, the signal is nondestructively sensed by the output structure and amplified to be read out.

The clock is a critical element of the CCD delay line operation. It must seamlessly input, transfer and output the electrical signal. The clocking circuit receives one master clock signal and continually outputs four overlapping and successive clock signals. Each of the four clock signals passes through a chain of inverters which serve as buffers to drive the capacitive load of the input structure, register body and output structure.

B. RESEARCH ACCOMPLISHMENTS

The primary research accomplishment of this thesis was determining how to design a bulk-channel CCD analog delay line for fabrication using the tools available at NPS, including the Magic design layout program and the Metal Oxide Semiconductor Integration Service (MOSIS) process. To accomplish this, a 64-stage, four-phase, bulk-channel CCD analog delay line with an on-chip clock generator and output amplifier was designed, developed, and implemented using CMOS VLSI. To support the primary goal, this research focused on 1) the transfer of charge packets along the CCD channel, 2) the electrode structure for achieving efficient charge transfer, and 3) the input/output circuits needed on the chip.

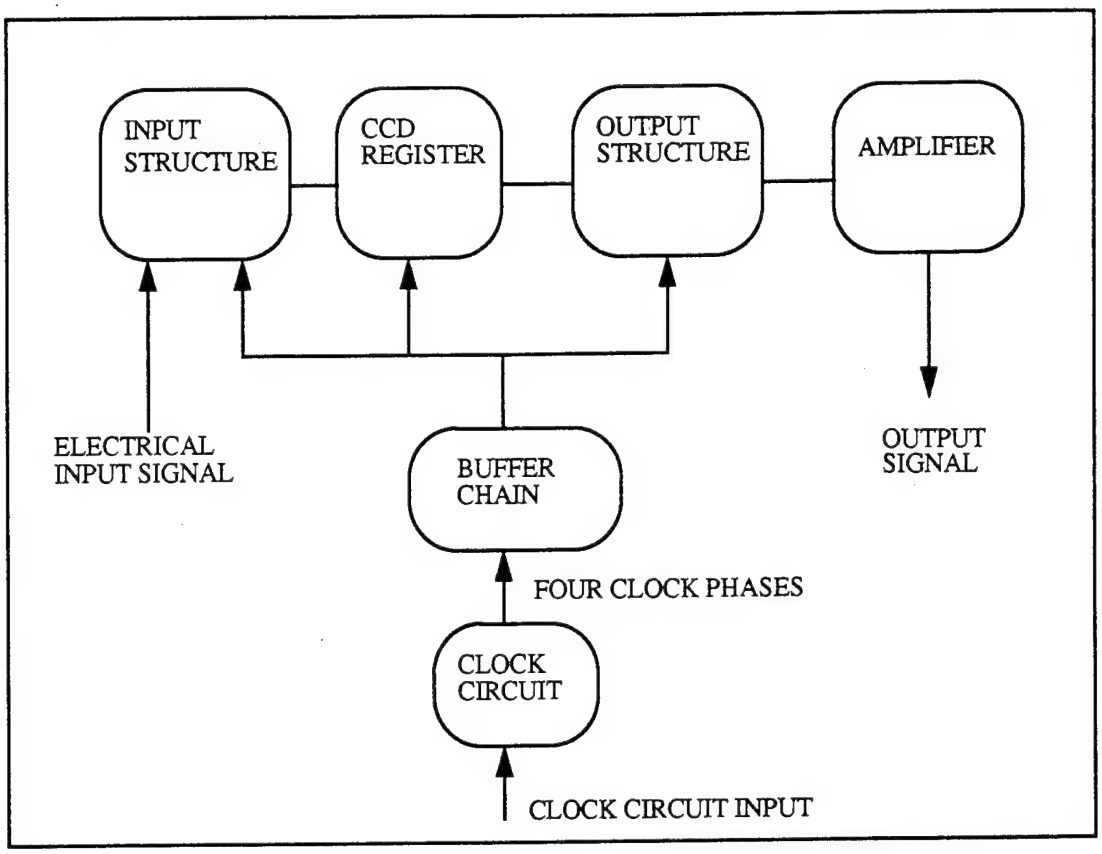

Figure 1. Block Diagram of CCD Analog Delay Line

The secondary goal of this thesis was to gain an understanding of the fundamental principles and operation of charge-coupled devices. Since there is currently no knowledge base of charge-coupled devices at NPS, a relatively long introduction is presented in this thesis. It is intended that the research material presented here, coupled with the List of References and Bibliography, will provide the foundation for any future research in this area.

C. REQUIRED HARDWARE AND SOFTWARE TOOLS

The design and layout of the Charged Coupled Device (CCD) Analog Delay Line chip was accomplished on the Naval Postgraduate School's Sun SPARC workstations. The

software tools included the VLSI CAD package which was developed by the University of California at Berkeley, and some commercially available programs.

1. Sun SPARC Workstation

The Sun Microsystems SPARCstation IPX is a UNIX based desktop computer with high-speed color graphics capability. The IPX operates at 40 MHz and is equipped with up to 64 Megabytes of RAM with 64 Kilobyte write-through cache, and 424 Megabytes of internal fixed disk storage; several large file systems are mounted by the IPX from a remote server.

2. Magic

All of the circuit layouts completed for this thesis were accomplished using the CAD tool Magic, which is an interactive editor and layout tool for designing Very Large Scale (VLSI) circuits. Since Magic operates on many types of UNIX based machines, it runs well on the Sun SPARC IPX with an integrated color monitor. In Magic, one can build simple cell layouts using a mouse or graphics tablet, or choose basic cell layouts in the program's cell library. These simpler cell layouts can be combined into larger structures, or even into completed integrated circuit layouts. Magic contains an interactive design rule checker which constantly checks the cell/circuit layout during the design process to verify all layout rules are obeyed. As a means of interfacing with other design programs, Magic can extract a layout to the native language of other simulation programs found in the Berkeley VLSI CAD package. Magic only permits Manhattan style designs, which are those with either horizontal or vertical structures; no diagonal or curved structures are permitted in Magic. There are many additional features of Magic that are too numerous to mention here. The reader is encouraged to consult the users manual for additional features and attributes of Magic [Ref.1].

3. B2 Spice

A fully integrated and interactive program, B2 Spice aids in the design of analog circuits in performing dc analysis, ac small-signal analysis, and transient analysis. B2 Spice is an analog circuit design and simulation program based on the numerical algorithms and formulas of SPICE, the standard for general purpose circuit simulation

developed the University of California at Berkeley. It can also be used to provide basic plotting of circuit parameters and circuit behavior. Although B2 Spice is a powerful tool in observing how circuits act, we made limited use of it; large circuits can require hours to simulate, and it cannot directly simulate a CCD circuit, only its peripheral circuitry.

4. B2 Logic

B2 Logic is a digital circuit design and simulation program. A network editor, network compiler, and digital circuit simulator are all integrated into one program. B2 Logic is a fully integrated and interactive program. It allows one to easily create and simulate sophisticated logic designs. Results can be obtained from a time line trace, output table, or an on-line probe. B2 Logic contains several device family libraries and it can check for fan-out violations and maximum pulse width violations.

5. Esim

Esim is an event- driven switch level simulator for NMOS and CMOS transistor circuits. Esim can be used to test or simulate the logical operation of a circuit design. After a circuit has been designed in Magic, it can be extracted into a format used by Esim, which is then used to monitor inputs, outputs, and nodes of interest setting or resetting their values. The 'watched' nodes can then be evaluated and the circuit checked for proper logical operation. There are numerous commands and options that may be used in the Esim simulation. The reader is encouraged to consult the users manual for additional features and attributes of Esim [Ref.1].

6. Ext2Spice and Ext2sim

Ext2spice and ext2sim read a file in the **.ext** format and create a new file in the **.spice** and **.sim** format respectively. The **.spice** file created by Ext2spice contains a list of transistors and capacitors. The designer must add the transistor models, in the form of Spice level 2 parameters, and other simulation information to produce and executable file in the **.spice** format. Ext2spice assumes transistor model names of nfet and pfet. This CAD tool sets the ground to node 0, Vdd to node 1, and node 2 is reserved as an error node. By labeling Vdd as 'Vdd!' and Ground as 'GND!', in the VLSI layout, the proper nodes will be assigned in the extraction. The .sim file created by Ext2sim is ready for use

by Esim. The Esim CAD tool assumes that the source voltage and ground are labeled 'Vdd' and 'GND' respectively [Ref. 1].

7. HSPICE

HSPICE is an optimizing analog circuit simulator by Meta-Software used for the circuit simulation of the VLSI circuit design. HSPICE is used for the steady-state and transient simulation of the circuit design. HSPICE program is compatible with most SPICE variations, has superior convergence, accurate modeling, and hierarchical node naming and references. Once the layout is complete using Magic, the design is extracted using the Ext2spice CAD tool. The designer must then add the transistor models, voltage sources and simulation information. The Graphical Simulation Interface (GSI) is used to graphically display the waveforms at various nodes in the VLSI design to ensure proper functional operation and design layout [Ref. 2].

D. THESIS STRUCTURE

Chapter II begins with the terminology associated with charge-coupled devices. It then moves into the fundamental theory and applications of CCDs. Detailed design considerations of the CCD delay line structure, especially the input and output structures, are presented in Chapter III. The CMOS layouts of the CCD circuit are shown in Chapter IV. A proposed testing methodology for the CCD Analog Delay Line designs are covered in Chapter V. Chapter VI outlines the thesis conclusions and further recommendations. Appendix A examines the development of the on-chip clocking circuit. Appendix B covers the development and simulation of the clock output driver circuit. Appendix C discusses the active-load differential amplifier which boosts the CCD output signal.

II. STRUCTURE & OPERATION OF CHARGE-COUPLED DEVICES

A. DEFINITION OF TERMS

The following terms are typical definitions related to charge-transfer devices that are currently in use.

1. Device Names

a. Charge-Transfer Device (CTD)

A device whose operation depends on the movement of discrete packets of charge along or beneath the semiconductor surface. Charge-Transfer Devices are of two types: Charge-Coupled Devices and Bucket-Brigade Devices.

b. Charge-Coupled Device (CCD)

A charge-transfer device that stores minority or majority carriers in potential wells and transfers this charge as a packet by translating the potential minima.

c. Bucket-Brigade Device (BBD)

A charge-transfer device that (1) stores charge as majority carriers in doped regions in the surface of a semiconductor that become reverse biased with respect to the substrate and (2) transfers this charge as a packet along the surface through a series of switching devices that interconnect the doped regions.

d. Bulk-Channel Charge-Coupled Device (BCCD)

A charge-coupled device that confines the storage and transfer of charges to a channel lying beneath the substrate surface, also called buried-channel charge-coupled device.

e. Surface-Channel Charge-Coupled Device (SCCD)

A charge-coupled device in which the potential wells are created at the semiconductor-insulator interface and charge is stored and transferred along that interface.

f. Multiphase Charge-Coupled Device

A charge-coupled device that requires more than one clock applied sequentially to provide directionality to the transfer of charge.

g. N-Channel Charge-Coupled Device

A charge-coupled device fabricated so that the charges stored in the potential wells are electrons.

h. P-Channel Charge-Coupled Device

A charge-coupled device fabricated so that the charges stored in the potential wells are holes.

i. Charge-Coupled Image Sensor

A charge-coupled device in which an optical image is converted into packets of charge that can be transferred as the electrical analog of the image.

2. General Terms

a. Charge Packet

A quantity of electrical charge that is the sum of the signal charge and bias charge (if used) and is stored in potential wells.

b. Charge Transfer Efficiency

The fraction of a charge packet successfully transferred from one electrode to the next electrode, denoted as η.

c. Depletion Region

That region in which the mobile carrier density is negligible compared to that of the majority carrier density in the bulk.

d. Drift-Aiding Fringing Field

An electric field at the semiconductor-insulator interface along the direction of charge propagation due to the potential on adjacent gate electrodes and the potential on the gate electrode directly above.

e. Empty Zero

A condition where there is zero circulating bias charge.

f. Fat Zero

Synonym for circulating bias charge, or background current, used to improve transfer efficiency.

g. Floating Diffusion

A diffused area into which a charge packet can be introduced, thereby changing its potential, typically used in detection schemes.

h. Floating Gate

An electrically floating gate on an insulating surface over an active portion of the semiconductor surface, typically used in detection schemes.

i. Gate Voltage

The voltage applied to the gate, or electrode, with respect to the substrate, often denoted by V_G.

j. Gate Electrode; Transfer Electrode

A conductor that is on an insulating surface over an active portion of the semiconductor surface and to which potential is applied.

k. Inversion Layer

That region in which the steady state condition minority carriers are present in concentration greater than that of majority carriers in the bulk.

l. Potential Well

A spatially defined depletion region of a charge-coupled device where a potential minimum exists.

m. Signal Charge

A quantity of electrical charge in a potential well that, in conjunction with the bias charge (if used), defines the signal level.

n. Threshold Voltage

The gate voltage required to create an inversion layer in the steady state case, denoted by V_T.

o. Transfer Channel

The area of a charge-coupled device in which the charge flow is confined.

B. THEORY OF OPERATION

The basic principle of charge transfer devices (CTD) involves the movement of information, represented by a quantity of charge, from one physical location of a semiconductor substrate to another in a controlled manner with the use of properly sequenced clock pulses. In other words, the device is basically a shift register; signal charges are stored and transferred in clocked shift register fashion under an array of closely spaced control electrodes. However, a unique feature of the CTD is that it will transfer analog signals, that can be introduced either electrically or optically. Thus, by providing suitable input/output circuitry and clocking waveforms, the CTD is capable of performing various functions such as analog delay line, serial memory for data storage, solid state imaging sensing, and logic operations.

As shown in Figure 2, charge transfer devices can be broken down into two subsets known as charge-coupled devices (CCDs) and bucket-brigade devices (BBDs). Charge-coupled devices can be further classified as surface charge-coupled devices (SCCDs) in which the signal charge is transferred along the Si/SiO_2 interface, or bulk charged-coupled devices (BCCDs) in which the signal charge is transported within the silicon substrate.

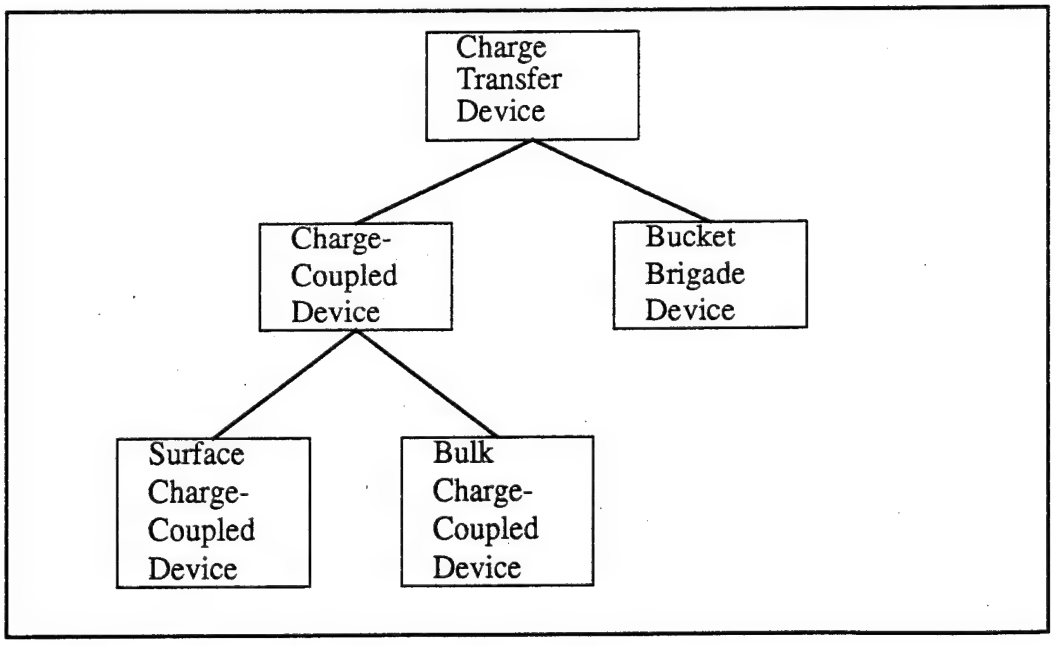

Figure 2. Family of Charge Transfer Devices

1. Basic Operation

CCDs operate by a mechanism of charge storage and transfer under an array of MOS control electrodes or gates. Information in the form of electric charge is transferred along the silicon/silicon dioxide surface or along the substrate in clocked shift register fashion by sequential manipulation of the voltages on the control electrodes that constrain this charge.

2. Charge Storage

The structure of a basic MOS CCD element (surface channel) is shown in Figure 3 (a). The silicon substrate is shown in the figures as being p-type, but n-type devices are also possible. Prior to the application of a positive voltage to the gate electrode, there is a uniform distribution of hole (majority carriers) in the p-type semiconductor.

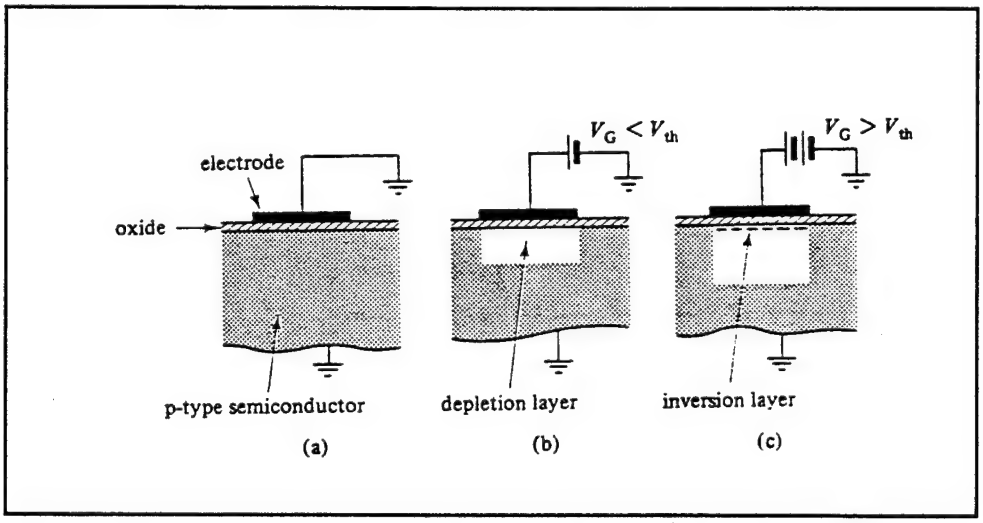

Figure 3. Single CCD Electrode, Showing Depletion & Inversion Layers. From Ref. [6].

The application of a positive voltage $+V_G$ to the electrode has the effect of repelling the positively charged majority carriers, the holes, in the silicon away from the vicinity immediately beneath the electrode. This region beneath the electrode becomes depleted of holes, as shown in Figure 3 (b). It is called a depletion region. For a given electrode structure and substrate doping concentration, the extent of the depletion region into the silicon is a function of the applied electrode voltage. As the gate voltage is

increased, the depletion region extends further into the bulk semiconductor, the potential of the semiconductor/insulator interface becomes increasingly positive. Eventually, a point is reached in which the gate voltage is so positive that electrons are attracted to the surface where they form an extremely thin (~$10^{-2}\mu m$) but dense inversion layer, as seen in Figure 3 (c). Information can now be stored in the depletion region in the form of minority carriers, electrons in this case. This charge may be introduce into the structure by either electrical or optical means, as discussed later.

In this example, a Surface Channel Charge-Coupled Device (SCCD), the stored electrons are localized at the Si/SiO_2 interface because they are attracted to the positive charge on the gate or electrode. The magnitude of the charge which may be stored under a given electrode is variable up to a maximum value that is dependent upon the electrode size and bias voltage. As the amount of charge stored is increased, the extent of the depletion region decreases in order to preserve overall charge neutrality in the system.

The potential well model, or fluid model, is another model that is sometimes more useful for describing the operation of a CCD; this model considers that the electrons are filling a potential well in the silicon substrate formed by the gate voltage, as seen in Figure 4. The potential well constrains the electrons to remain under the electrode. This can be shown from the energy-band diagrams shown in Figure 5 which represent the conditions shown in Figures 3. The potential minimum at the silicon interface is generally referred to as the surface potential, ϕ_S. The surface potential for an empty well, ϕ_{SO} (the depth of the potential well) can be derived from the MOS equations [Ref. 6]:

$$V_G - V_{FB} = \phi_{SO} + B\,\phi_{SO} \qquad (1)$$

where $$B = \sqrt{2\varepsilon\varepsilon_o q \frac{N}{C_{ox}}} \qquad (2)$$

and V_{FB} = flat-band voltage

$\varepsilon\varepsilon_0$ = silicon dielectric constant

q = electronic charge

N = substrate doping concentration

C_{ox} = oxide capacitance per unit area

When carriers are introduced into the well, the surface potential decreases as the inversion layer charge increases and a larger voltage drop appears across the SiO_2 insulator.

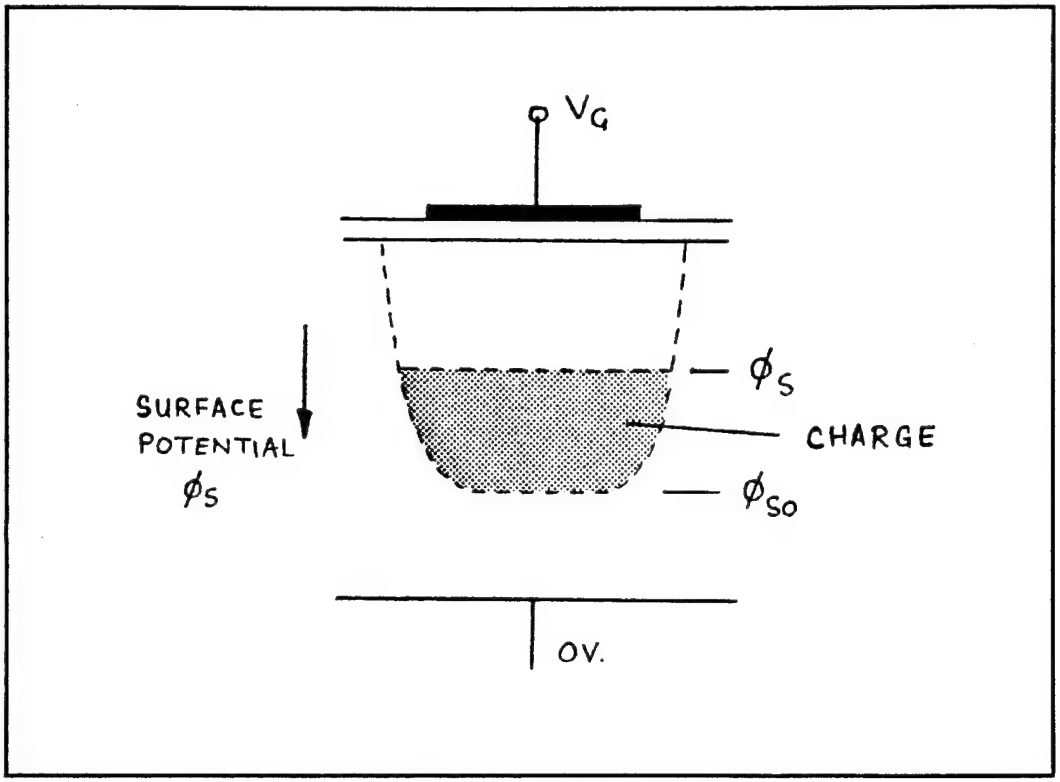

Figure 4. Potential Well Model.

The CCD is inherently a dynamic memory since the stored information disappears with increasing time. The mechanism for this is the thermal generation of electron-hole pairs which takes place in any semiconductor. This causes the depletion regions to be slowly filled with minority carriers which gradually mask the stored information.

3. Basic CCD Structure

The cross section of a typical CCD is shown schematically in Figure 6. The basic device consists of a linear array of closely spaced control gates, or electrodes, on a continuous silicon dioxide dielectric layer which covers the silicon substrate material. Charge

storage and transfer takes place in the channel region of the device, which may be bounded by high concentration channel-stop diffusions. The charge constrained in the depletion region beneath a given electrode is called a charge packet. For analog and electrical devices, charge packets are introduced by applying suitable voltages to a p-n junction at the input of the CCD. For optical imaging applications, they are formed as a result of electron-hole pair generation caused by light energy incident on the silicon substrate.

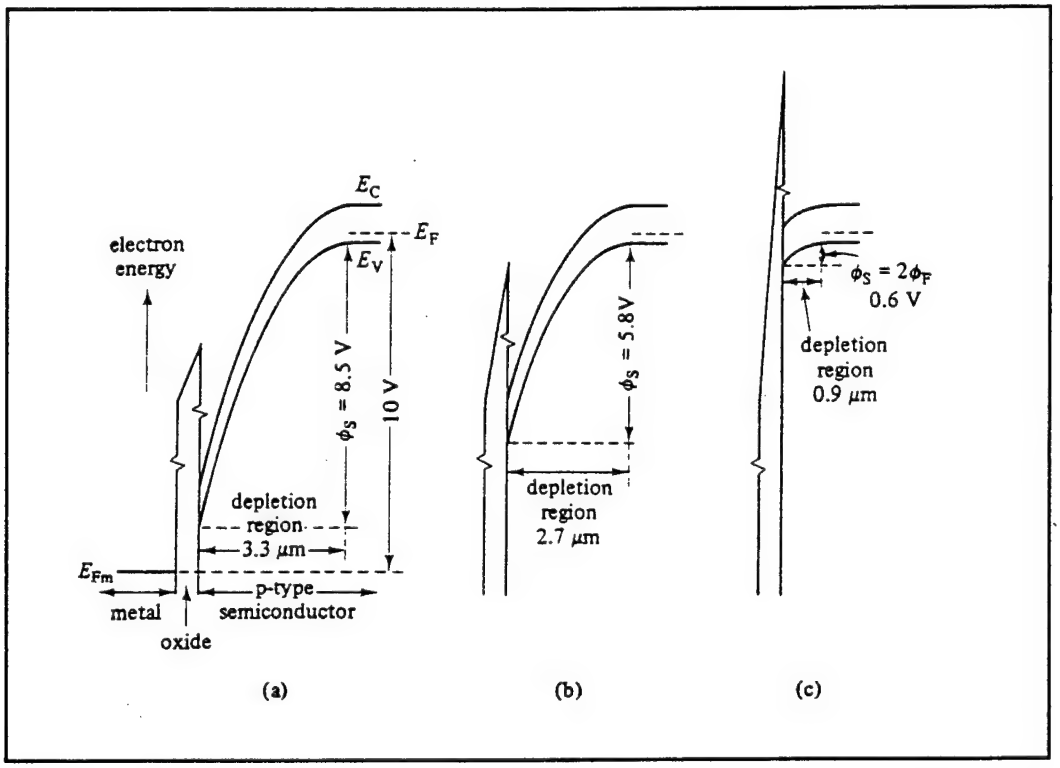

Figure 5. Energy-Band Diagrams for the MOS Structure Shown in Figure 2. (a) No charge in potential well; (b) Potential well approximately one-third full; (c) Potential well completely full - equilibrium. From Ref. [5].

4. Charge Transfer

Once a charge packet has been introduced to the CCD it may be moved through the structure in the manner illustrated by Figure 7. This figure also illustrates the required driving waveform, or clocking pulses.

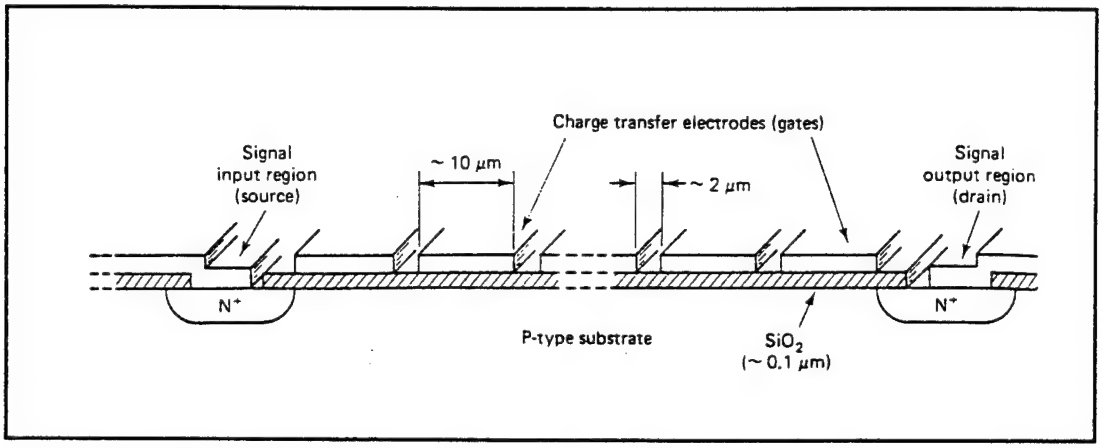

Figure 6. Basic Structure of a Charge-Coupled Device. From Ref. [12].

At time t_1, Figure 7 (a), a charge packet is held under electrode ϕ_2, the voltage of which is $+V_{CC}$. Electrodes ϕ_1 and ϕ_3 are held at a resting potential, $+V_{SS}$. At a later time t_2, in Figure 7 (b), electrode ϕ_3 is pulsed to $+V_{CC}$. This produces a depletion region under ϕ_3 which, because the electrodes are closely spaced, couples with that under ϕ_2, with the result that charge begins to move from under ϕ_2 to under ϕ_3. The voltage on ϕ_2 is then reduced to $+V_{SS}$ with a slowly falling edge. The voltage on ϕ_2 is not reduced to $+V_{SS}$ instantly because the charge carriers require a finite time to diffuse across the width of the electrode. Figure 7 (c) shows the charge transfer complete at time t_3, with the charge now stored in the depletion region under ϕ_3.

Note that ϕ_1 has to be kept at a low potential throughout to prevent backflow of charge. Thus, three electrodes are required to store and transfer one charge packet and,

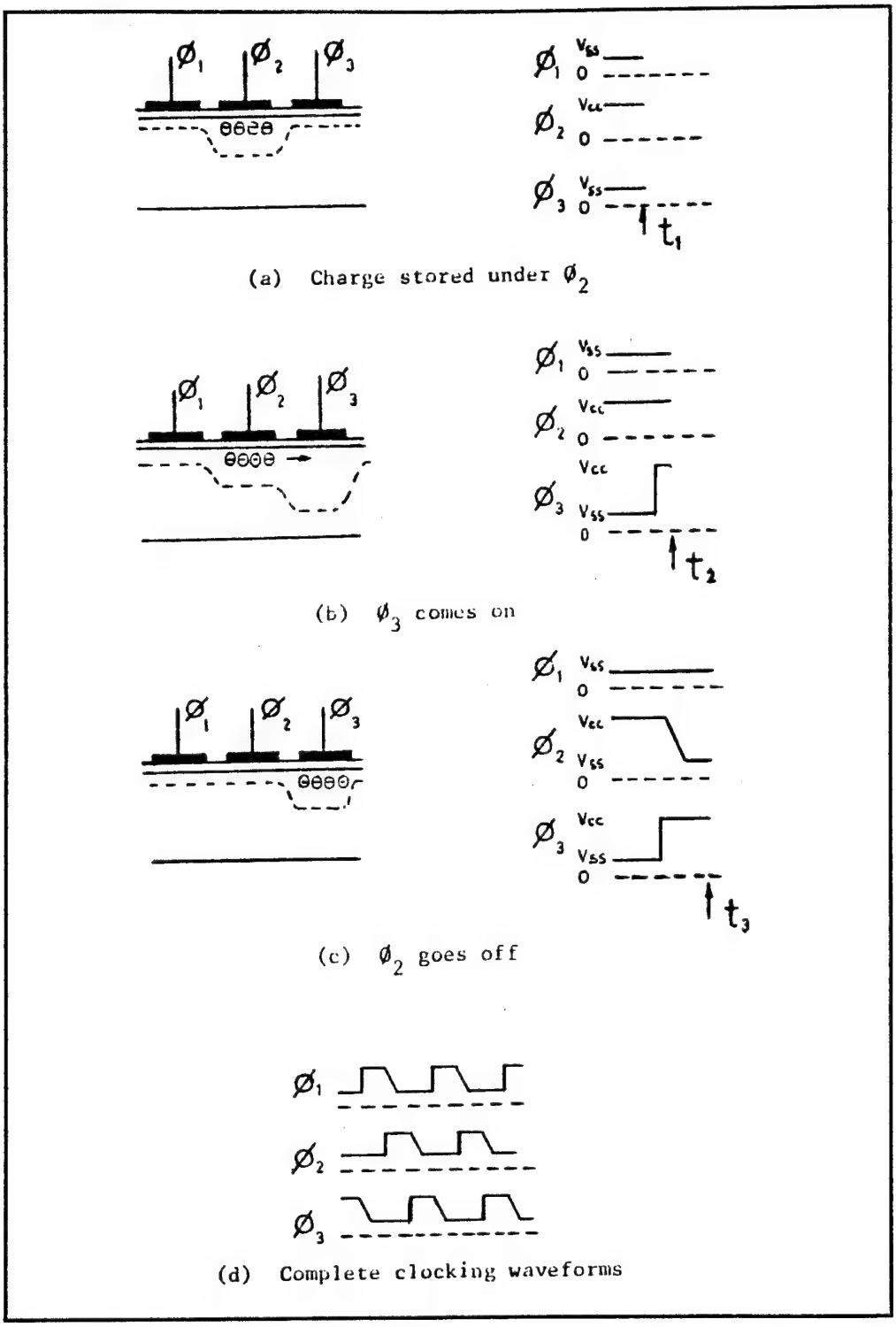

Figure 7. Charge Transfer for a Three Phase CCD.

as a consequence, are usually referred to as one element of the CCD. Thus, the electrodes of this CCD array are arranged in triplets and are connected sequentially to the drive line carrying the three-phase driving waveforms. Hence, continuation of the clocking sequence, as shown in Figure 7 (d), would result in the movement of the charge packet from under ϕ_3 to under the next ϕ_1, then to ϕ_2, and so on to the output of the array. Note that there can be a charge packet under every third electrode in this array and that application of drive pulses causes these charges to be moved simultaneously.

For correct operation of the CCD, it is generally necessary to maintain the silicon surface in depletion at all times; this is the reason for using the resting voltage $+V_{SS}$. If V_{SS} is applied as a bias to the substrate, which is common to all electrodes, the generation of the clock pulses is greatly simplified.

5. Charge-Transfer Efficiency

The fraction of charge that is correctly transferred from one well to the next is referred to as the charge transfer efficiency, η. The small fraction of charge left behind at each transfer is the transfer loss, or transfer inefficiency, denoted by ε ($\eta + \varepsilon = 1$), where $\varepsilon << 1$. Because η determines how many transfers can be made before the signal is seriously distorted and delayed, it is a very important figure of merit for a CCD. If a single charge pulse with an initial amplitude P_o is transferred down a CCD register, after n transfers the amplitude P_n will be:

$$P_n = P_o \eta^n \approx P_o (1 - n\varepsilon) \quad \text{for small } \varepsilon \qquad (3)$$

Therefore, ε must be very small if a large number of transfers are required. If we allow an $n\varepsilon$ product of 0.1, an overall loss of 10 percent, then a 4-phase, 250 stage shift register requires $\varepsilon < 10^{-4}$, or a transfer efficiency of 99.99 percent.

There are two major causes of transfer inefficiency:

a. Incomplete charge packet transfer due to the fact that the carriers require a finite time to diffuse from under one electrode to the next. As the spacing between electrodes is reduced the effect becomes smaller but this mechanism imposes an upper limit on the speed at which the device can be operated. The lower CCD transfer speed limit is

set by the thermal carrier diffusion effect which is described in the next section.

b. The effect of carrier trapping states which are largely localized at the Si/SiO_2 interface. As a charge packet arrives at a storage electrode, a small portion of it is instantly "trapped" by the interface states under that electrode. When the packet is moved on, the states will empty into trailing packets, thus giving rise to small residual charges trailing behind the main packet. This effect of interface states is more pronounced in surface channel devices. The trapping of charge by the interface states can largely be avoided by means of bulk-channel construction [Refs 4 & 5].

6. Free-Charge Transfer Mechanism

Three separate mechanisms cause the free charge to move from one well to another: self-induced drift, thermal diffusion, and fringing field drift [Refs. 3 & 5].

a. Self-Induced Drift

Self-Induced Drift is a charge-repulsion effect which is only important at large signal charge densities ($\geq 10^{10}$ charges/cm^2). The mechanism is important in transferring the first 99% or so of the charge signal and is responsible for improving the frequency response of certain devices operating with a large background charge, or "fat zero". [Ref.5]

b. Thermal Carrier Diffusion

Thermal carrier diffusion, which dominates the remaining 1% of signal charge transfer in SCCDs, gives an exponential decay of the amount of charge under the transferring electrode. The decay time constant is proportional to the square of the gate length:

$$\tau_{th} = L^2 / 2.5\ D \qquad (4)$$

where L is the center-to-center electrode spacing and D is the diffusion constant; therefore, this effect becomes increasingly important at longer gate lengths (typically 8 -10 μm) [Ref. 5].

By means of thermal carrier diffusion alone, 99.99% of the charge could be transferred each cycle at frequencies f (in Hz) given approximately by:

$$f = 5.6 \times 10^7 / L^2 \qquad (5)$$

assuming D = 6.75; L is center-to-center spacing measured in μm.

c. Fringing Field Drift

Fringing field drift can help to speed up the charge transfer of the remaining 1% in BCCDs considerably. The fringing field is the electric field along the direction of the charge propagation along the channel. This field will vary with distance along the gate with the minimum occurring at the center of the transferring gate. The magnitude of the fringing field increases with increasing oxide thickness and gate voltage. It decreases with increasing gate length and doping density and, in general, is higher in bulk channel devices. The fringing field lines become increasingly steeper and more effective as the channel is moved further away from the oxide/silicon interface [Ref. 5]. The effect of the fringing field upon charge transfer is difficult to assess analytically. A computer simulation of the transfer process under the influence of strong fringing fields has indicated that the charge remaining under the transferring electrode still decays exponentially with time [Ref. 5].

C. APPLICATIONS OF CHARGE-COUPLED DEVICES

1. Charge-Coupled Imagers

The CCD concept introduces a revolutionary new approach to the design of self-scanned solid-state image sensors. One can think of the CCD as the semiconductor equivalent of an electron-beam tube in which the charge signal can be moved or transferred and stored under the control of the clock voltage pulses free of pick-up and switching transients. The only limitations on the charge-coupling process comes about because the charge transfer is not 100% complete. The finite transfer loss results in some distortion of the signal, and introduces transfer noise.

a. Line Imagers

Two line imagers shown in Figures 8 and 9 illustrate the ways in which an

optical signal can be detected. We will now assume that an optical input is applied to one of these CCD registers while the clock voltages are adjusted so that one potential well is created at each stage along the CCD channel. The photo-generated charge will collect in these wells during the optical integration time. At the end of the integration time, the accumulated charge packets representing the integrated optical input are shifted down the

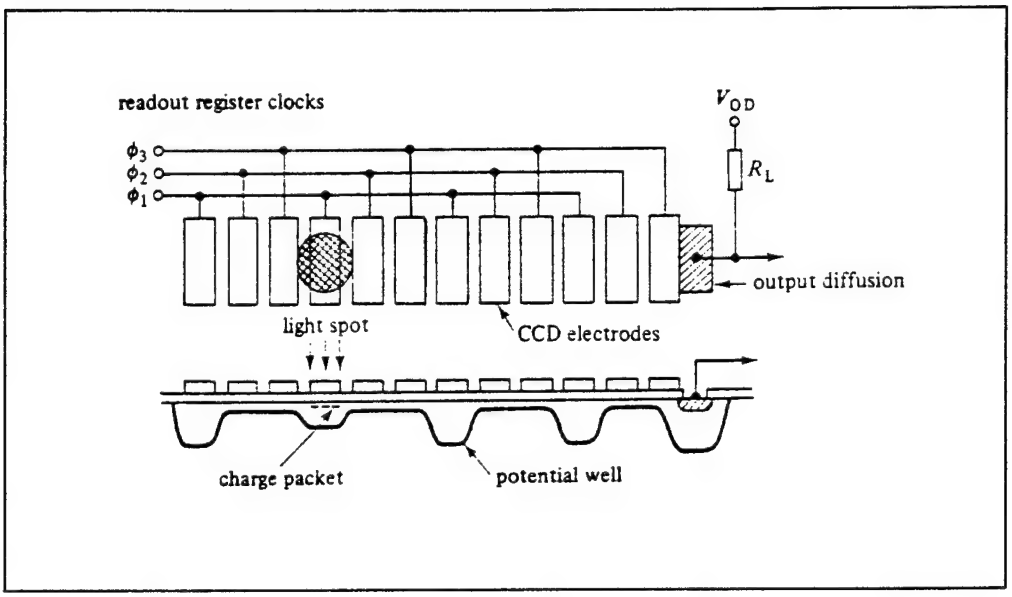

Figure 8. Basic Principal of CCD Imaging. From Ref. [6].

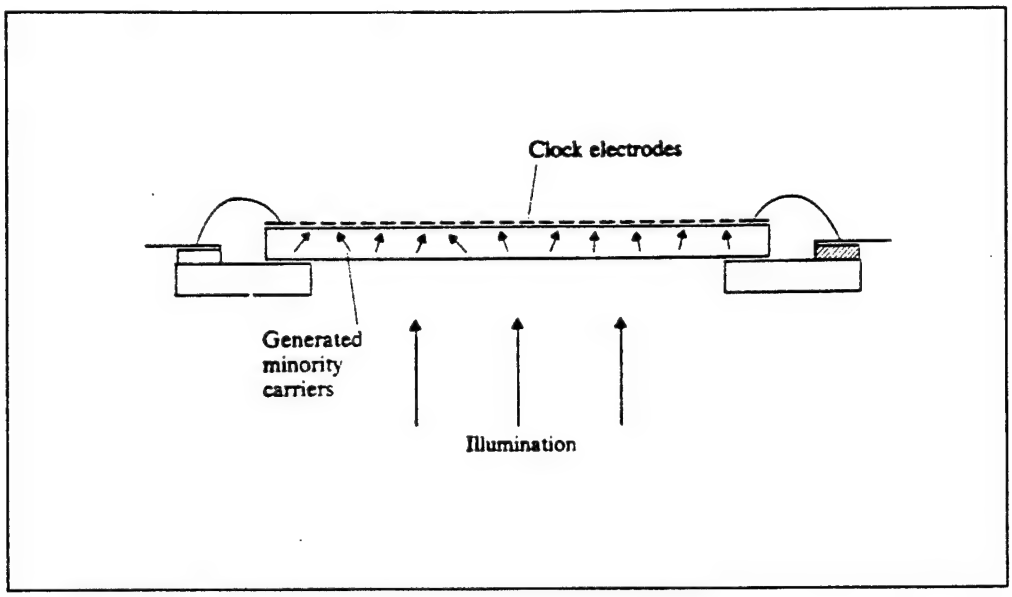

Figure 9. CCD Imager Using Back-Surface Illumination. From Ref. [7].

charge-coupled imager register and detected by a single output amplifier. To prevent smearing of the image, the optical integration time should be much longer than the total time required to transfer the detected image from the CCD line sensor. Since all charge elements are amplified by the same amplifier, non-uniformities, such as those found in optical arrays, are avoided. Since there is no direct coupling of the clock voltages to the charge signal in the CCD channel, the clock pick-up is limited only to a single output stage. In addition, since only the clock frequency is used in CCD transfer, clock pick-up is not the problem as it is in x-y scanned arrays where one of the clocks occurs at the horizontal line frequency and cannot be simply removed by appropriate filtering.

b. Area Imagers

The two most popular area charge-coupled imagers are the interline transfer system and the frame transfer system, shown in Figures 10 and 11, respectively. The interline transfer system can be visualized as consisting of a parallel array of the line sensors with non-illuminated registers all leading in parallel into a single output register. The optical image is detected by vertical lines of photosensitive MOS capacitors formed by a transparent polysilicon photogate. The vertical line sensors are separated from each

other by opaque vertical CCD registers. Since two photosensor elements can be read by one stage of the vertical register, the image is detected as two vertically interlaced fields. Once every frame time one field is transferred into the non-illuminated registers. Then, the entire detected image is shifted down in unison by clock A and transferred into the output register one horizontal line at a time. The horizontal lines are then transferred out from the output register by the high frequency clock B before the next horizontal line is shifted in.

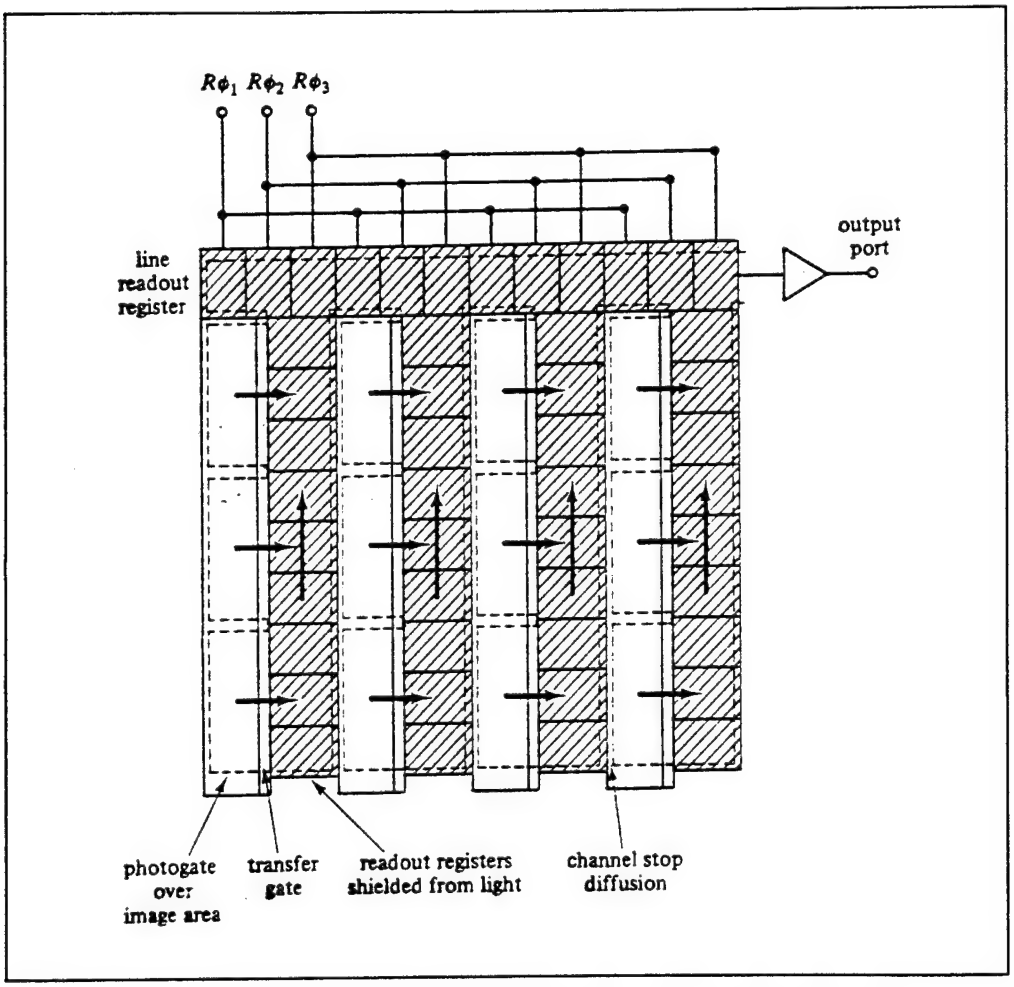

Figure 10. Interline Transfer Array Schematic. From Ref. [6].

The frame transfer system that can be illuminated either from the tip or from the back of the substrate is shown schematically in Figure 11. In this system the optical image is detected by a separate photosensitive area of CCD registers. Then, the detected image is transferred into the opaque temporary storage array by clocks S and I during the vertical blanking time. From there, it is shifted down one horizontal line at a time into the output register and transferred out by the high speed clock R. The time available for parallel loading of the output register corresponds to the horizontal line retrace time.

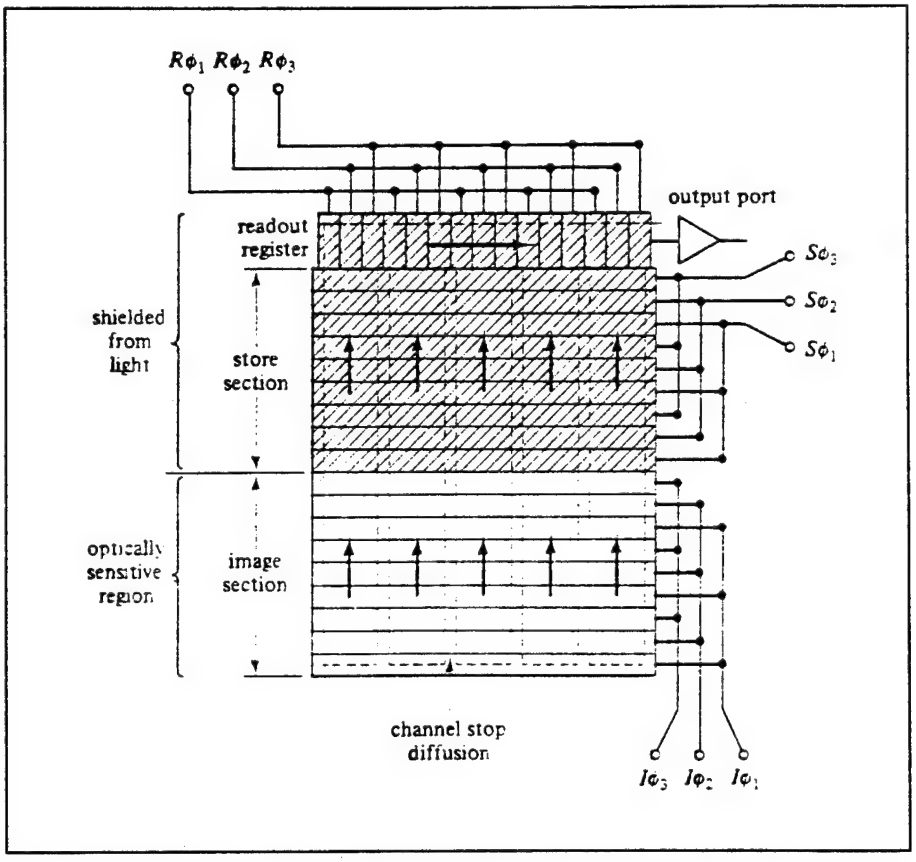

Figure 11. Frame Transfer Array Schematic. From Ref. [6].

2. Digital Memories

Charge-Coupled shift registers are basically analog devices. To store digital signals in these devices it is necessary to periodically refresh, regenerate, or redigitized the charge signals. Floating diffusion or floating gate output can be used for construction of

signal regeneration stages. Signal refreshing stages can be constructed following procedures similar to those used in the construction of the refreshable MOS memories.

The simplest type of CCD memory organization is shown in the block diagram of Figure 12. In this simple arrangement, information in the form of charge packets are transferred through each memory cell until it reaches the output sense amplifier. From there the charge packets are either recirculated or are read out; if read out, then new charge packets are serially entered at the input.

From the CCD memory description, it becomes apparent that a big advantage of random access memory (RAM) over CCD memory is its faster access time for almost any bit of data. In a RAM, each memory location is individually and directly addressed, but access time for a bit of data in a CCD memory depends upon its location in the memory block. Data that is near the output is available quickly, but data that has just been entered must transfer through the entire memory block before it can be accessed. For a comparison, the mean access time for a 4k-bit CCD memory block at 5 MHz is about 400 μsec, while the mean access time for a comparably sized MOS RAM is just 1 μsec. [Ref. 6]

There are four possible memory organizations using the CCD: the serpentine structure shown in Figure 12; the loop organization, which is similar to the serpentine; the Series-Parallel-Series (SPS) memory design; and the Line Addressable Random Access Memory (LARAM) design. Detail on these memory designs can be found in Refs [3] and [7].

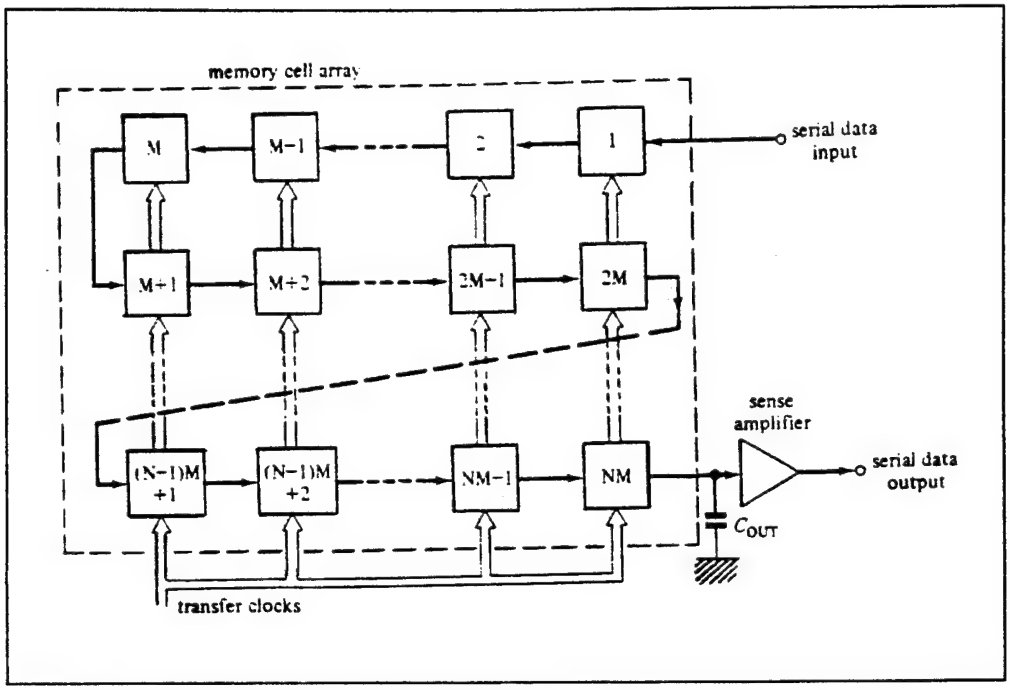

Figure 12. Block Organization of CCD Memory. From Ref. [6].

3. CCD Logic

In addition to their potential use in memory applications, CCDs can be used to implement digital logic. Their high packing density and good signal charge isolation make them attractive for this application. In CCD logic, a logical 1 is represented by the largest charge packet that can be held under the storage electrode while a logical 0 is represented by the absence of charge. A 2-input OR/AND gate structure using a 2-level, two-phase electrode gate is shown is Figure 13. More detailed information regarding the use of CCDs for logic applications can be found in Refs [6] and [7].

4. Analog Signal Processing

Charge-coupled devices present another technique for processing analog information. CCDs may be cheaper than digital filters for some applications because (1) CCDs eliminate the need for analog-to-digital and digital-to-analog conversion, and (2) a single CCD filter operating as a function unit can replace a large amount of digital hardware.

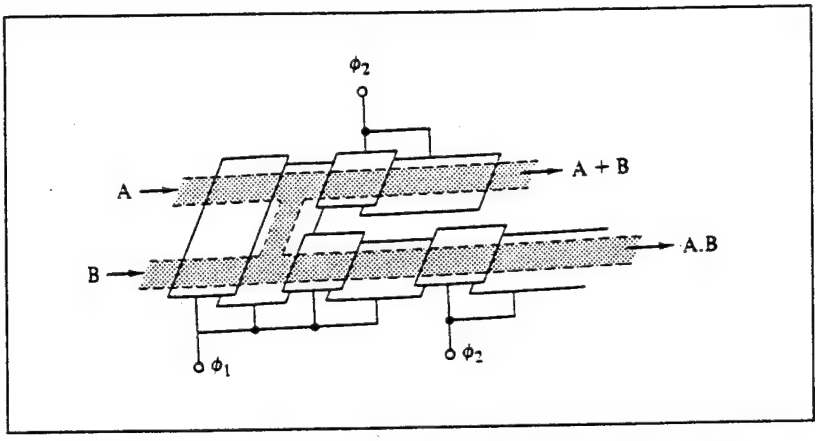

Figure 13. 2-Input OR/AND Gate Utilizing a Two-Phase CCD. From Ref. [6].

a. Delay Line

One of the most direct applications of CCDs is in fixed or electronically variable delay lines. The time delay, τ_d, for a CCD delay line is

$$\tau_d = N\,(1 / f_c) = N / (2\,\Delta B), \qquad (6)$$

where N is the number of stages, f_c is the clock frequency, and ΔB is the bandwidth. The CCD delay line operates by sampling the input signal once every clock cycle. Therefore, it is capable of signal bandwidth ΔB, close to $f_c / 2$. The electronically-variable delay is obtained by varying the clock frequency. The maximum time delay, τ_{dmax}, for a CCD delay line is independent of the number of stages. The practical upper limit for τ_{dmax} at room temperature is 0.1 to 10 seconds. For example, audio delay of 10 to 20 ms with ΔB of 20 kHz would require f_c = 40 kHz and N = 400 to 800 stages.

b. Transversal Filters

Transverse filters with either fixed or variable weights have been implemented using CCDs for processing of analog signals. The signals at each stage of a CCD delay line can be tapped, weighted, and summed by a technique illustrated in Figure 14, which is referred to as the electrode weighting and summing approach. Specific CCD implementations of transversal filters with fixed weights, using electrode weighting and summing, that have been already considered include match filters for various

trum communication applications, radar pulse compression band-pass filters, and chirp-z transform filters. [Ref. 8]

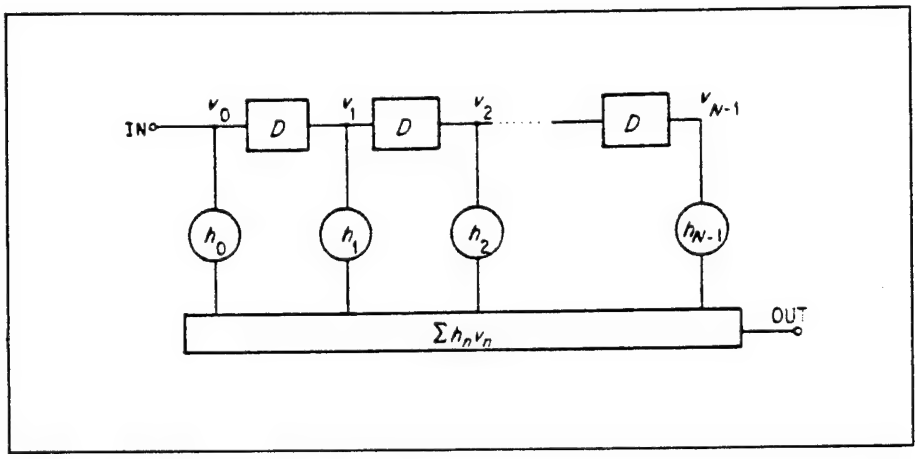

Figure 14. Block Diagram of a Transversal Filter. From Ref. [3].

III. CCD DELAY LINE DESIGN

A. CCD STRUCTURE

1. Bulk Channel versus Surface Channel

As discussed in Chapter I, CCDs can be classified as surface channel charge-coupled devices (SCCDs) or bulk-channel charge-coupled devices (BCCDs) depending on whether the charge is transferred at the silicon surface or within the bulk of the silicon substrate. A SCCD, in its simplest form, consists of a linear array of MOS capacitors fabricated on an oxidized p-Si substrate of uniform doping as shown in Figure 6. As explained in Chapter II, charge transfer takes place along the Si/SiO_2 interface, which results in a portion of the charge being trapped by interface states under the electrodes, thus decreasing charge transfer efficiency.

In BCCDs, a shallow n-layer is placed under the oxide layer, which causes the potential well minima occur within the Si bulk, so that the mobile electrons are not in contact with the oxide/semiconductor interface. This results in a transfer efficiency improvement for two distinct reasons. First, when compared to SCCDs, the BCCD channel displays considerably lower charge trapping and consequently better transfer efficiency. Second, during charge transfer, lateral fringing electric fields caused by unequal adjacent gate voltages introduce a significant drift force which moves charge from one bucket to the next very efficiently [Ref 5]. BCCD transfer speed is dominated by fringing field drift, while SCCD transfer speed is dominated by the relatively slower thermal carrier diffusion. As a result, BCCDs' clock transfer speeds are up to an order of magnitude higher than comparable SCCD clock speeds. A disadvantage of the BCCD design is that it can only contain about 25% of the maximum charge of a comparable SCCD.

For this project, only bulk-channel CCDs were attempted, as MOSIS design rules only allow BCCDs to be laid out.

2. Electrode Material

a. Single Metal Gates

The simplest CCDs were fabricated with single level metal gates, usually

aluminum because of its very high conductivity. These aluminum gates had gaps of 2 or 3 μm between them. However, too large of an inter-electrode gap can create a potential barrier between adjacent wells, which inhibits charge transfer. While the first CCDs were of this type, the requirement for very small gaps or no gaps between the gates, and the instabilities associated with the exposed channel oxide in the gaps, lead to the development of more reliable sealed structures as described below.

b. Conductive Channel

The conductive channel is a single level technique that uses undoped polysilicon as a high resistivity dielectric in the gap regions to eliminate the effects of static charge on the oxide and to minimize potential energy barriers between adjacent wells by grading the potential between wells. In one variation of this method, undoped polysilicon is deposited over the electrode and gap regions. The electrodes are then defined by selective doping of the polysilicon. In another variation, a thin (50 nm) undoped polysilicon layer is deposited over the entire channel region and metal electrodes are located on this layer. One problem with this system is the difficulty in maintaining adequate resistivity in the polysilicon layer. If the resistivity is too low, the power dissipation is increased due to leakage between clock lines. If the resistivity is too high, the potential in the gap lags behind that of the clock lines and thus reduces the effectiveness of this system.

c. Polysilicon-Aluminum Gates

Polysilicon-aluminum gates represent a self-aligning, overlapping gate structure in which the separation between the gates is formed by thermally grown SiO_2, typically 0.1 to 0.2 μm thick, and corresponds to the thickness of the channel oxide. This gate structure can be used for construction of two-phase as well as four-phase CCDs. One of the limitations of this approach, that is common to all polysilicon gate structures, is that the polysilicon RC time delay, due to the high resistivity of the polysilicon, is much larger than that of aluminum. This RC time delay disparity can cause timing problems.

d. Polysilicon-Polysilicon Gates

With a choice between aluminum or polysilicon gates for an electrode gate material, polysilicon is preferable for the following reasons: the SiO_2 insulation layer

grown by thermal oxidation directly on the polysilicon electrode is conformal to the gate profile and is of high integrity; completely sealed, stable electrode structures are possible; and the semi-transparent nature of the polysilicon facilitates the design of optical imaging arrays [Ref. 9].

Polysilicon-Polysilicon Gates is an outgrowth of the Polysilicon-Aluminum Gate structure. In this configuration, the RC time delay disparity between polysilicon and aluminum gates is eliminated. With this gate structure, aluminum metallization is necessary for interconnections and bonding pads.

Two-level polysilicon structure requires relatively simple processing techniques but also has its disadvantages. Since the gates overlap, the size of the storage well is determined by the first layer of polysilicon, which is relatively large compared to a triple layer structure. There is a need to use small contact holes and short circuits in the polysilicon are fatal because electrodes on the same level are connected to different phases. Despite these disadvantages, the use of a two-level polysilicon-polysilicon structure is attractive for this device fabrication because these technologies are closest to those used to fabricate conventional CMOS integrated circuits.

e. Triple-Polysilicon Gate Structures

Triple-polysilicon gate structures can be used to fabricate sealed-channel multi-phase CCDs. Unlike double polysilicon gate structures, the size of two of the potential wells in the triple polysilicon gate construction is subject to alignment tolerances. The main advantages of the triple-polysilicon construction are that for a given gate size, the spaces between the gates become minimized; the shorts between the gates on the same polysilicon level do not lead to catastrophic failures; and there is no need for small contact holes between the polysilicon gates and the aluminum interconnections as for most CCD structures. This process can also provide the smallest desirable gate size. Unfortunately, the three-level polysilicon electrode technology requires a more complex fabrication process, which MOSIS does not accommodate.

3. Channel Confinement

Various electrode structures which produce unidirectional signal charge flow along the silicon-oxide interface or in the bulk have been examined. However, an important problem deals with the confinement of the signal charge within the channel region so that it is not lost from the lateral edges of the channel. There are three different methods used to define the width of the CCD channel and assist in lateral charge confinement.

a. Thick Field Oxide

Thick field oxides, shown in Figure 15 (a), (1-2 μm) are useful for {111} n-type material but not for {100} Si because to obtain field threshold voltages compatible with normal clock voltages, the oxides required are too thick to permit precise photoresist patterning. It has been found that with high resistivity substrate material, the thick oxide technique provides only a weak definition of the channel and its width will change significantly with gate voltage and the amount of charge in the potential well. Magic does not allow thick field oxide design.

b. Diffused Channel Stop

A second approach to lateral channel confinement is the use of a channel stop diffusion as shown in Figure 15 (b) and 16. Although this technique requires additional masking and process steps, it is the best technique because it strongly clamps the surface potential which defines the extent of the channel more precisely. Useful for both surface and bulk channel devices, the diffused channel stop method eliminates the need for extremely thick field oxides.

c. Electrostatic Field Shield

The third approach is the use of an electrostatic field shield as shown in Figure 15 (c). In this technique the field region is covered by a relatively thin field oxide on which a doped polysilicon layer is deposited. The polysilicon is then oxidized and may then be covered with other electrodes. With proper biasing of the polysilicon layer with polarity opposite to that applied to the CCD gates, a strong accumulation region forms on the silicon surface preventing channeling. This technique is not normally used for CCDs

because of the restriction on device layout that it imposes with the need to interconnect each part of the shield to a bias voltage.

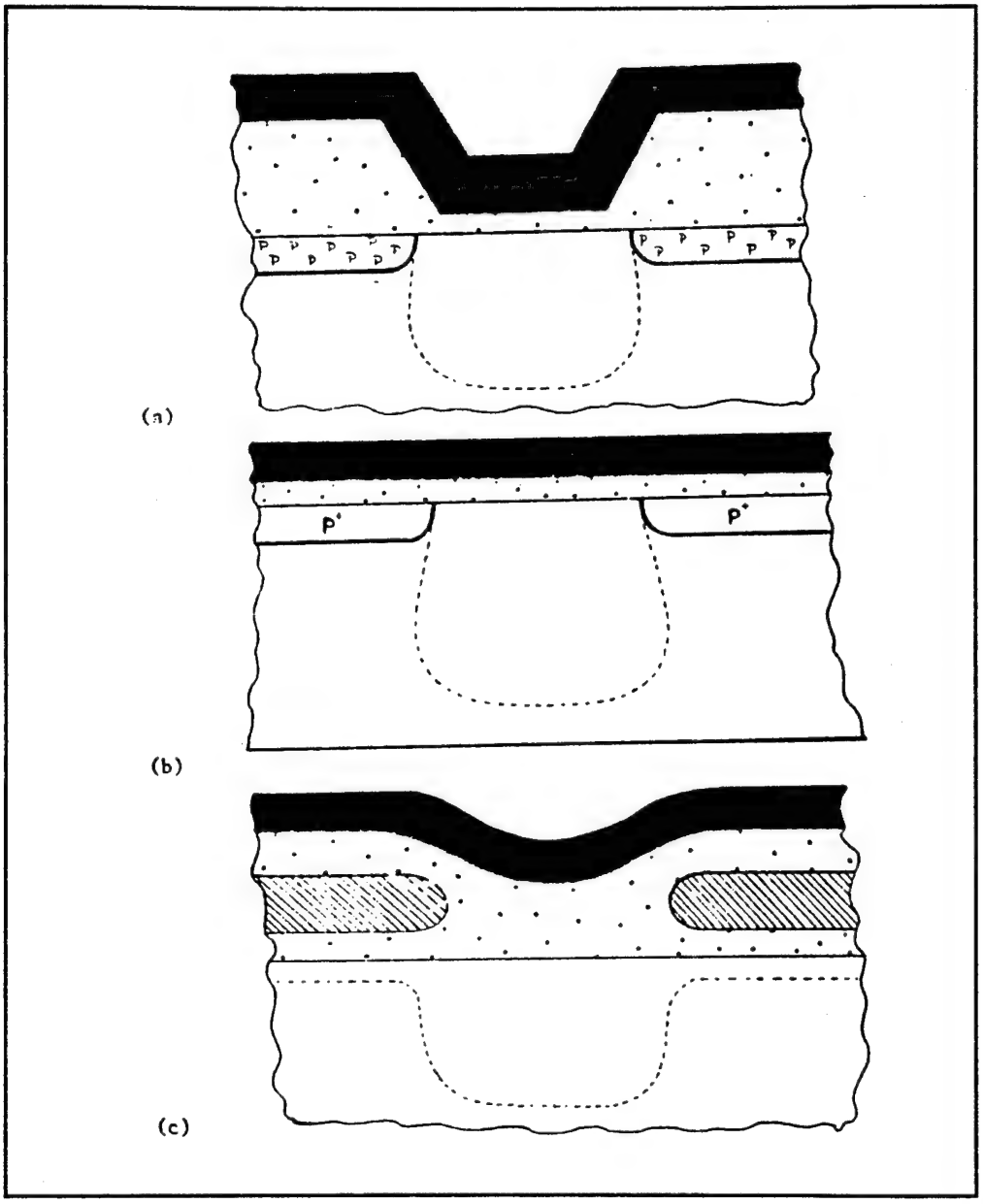

Figure 15. Lateral Channel Confinement Techniques. From Ref. [4].

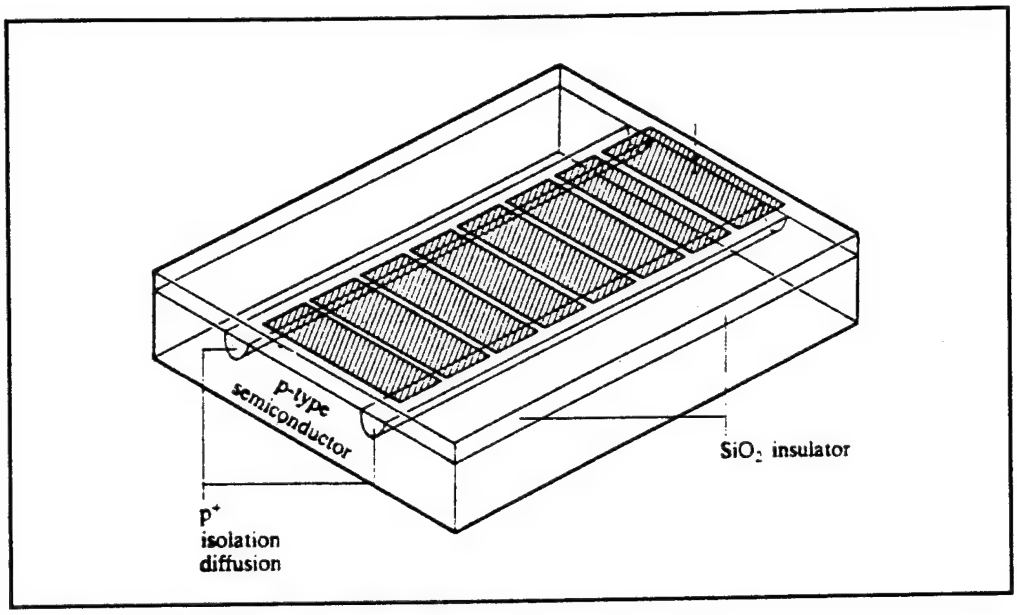

Figure 16. Channel Stop Diffusion. From Ref. [7].

4. Number of Clock Phases

As was discussed in Chapter II, a CCD transfers charge along a channel created by pulsing a series of transfer electrodes with properly phased voltages. Transfer schemes have been proposed involving from one-to-four-phase systems with a variety of electrode structures. For a p-phase system, there are p storage electrodes per unit cell, and p transfers per unit cell. In order to clock signal charges through the cells at clock frequency f_c, the transfer rate between individual electrodes must be pf_c or the maximum allowable transfer time per electrode is $1/pf_c$.

a. Three-Phase Systems

Three- (or more) -phase systems are required to control the direction of charge-transfer if simple symmetrical electrodes are used. While one potential well is being emptied of charge, another is receiving the charge and a third is blocking the backward flow of charge. A description of charge transfer for a three-phase CCD was presented in Chapter II.

Three-phase systems were the first to be developed and were used extensively in early CCDs. Three-phase systems, shown in Figure 17, have relatively large signal handling capability and do not require any special fabrication technology. However, there are problems associated with crossovers required in a three phase system. Additionally, three-phase systems have relatively large cell-space requirements and the three-phase clock is awkward to implement.

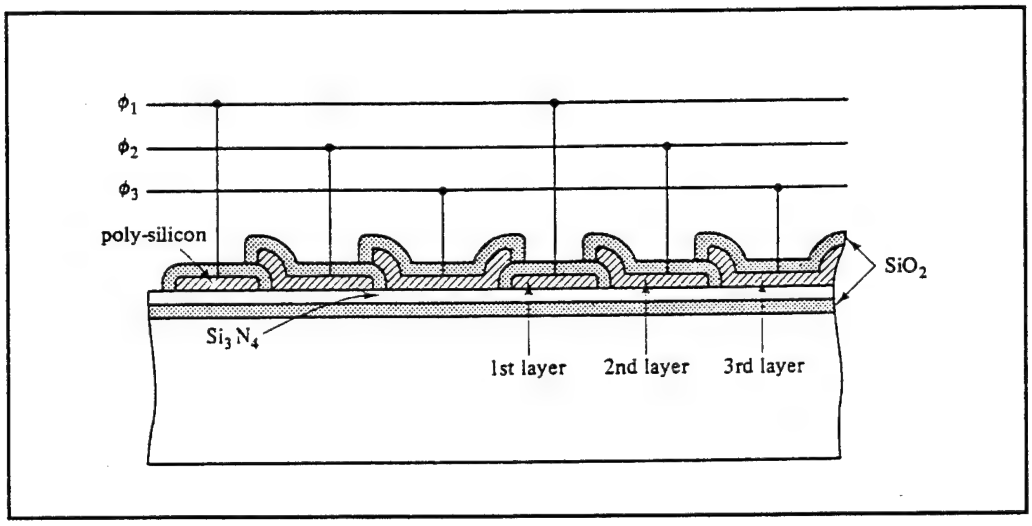

Figure 17. Three-Phase Structure. From Ref. [6].

b. Two Phase Systems

For CCDs with symmetrical potential wells it takes clocks with three or more phases to determine the directionality of the signal flow. However, if the potential wells are made directional by designing some asymmetry into the CCD cells, such as a built-in electric field, a two phase CCD can be constructed. Two techniques for accomplishing this are illustrated in Figure 18. The objective of both techniques is to increase the potential difference across the oxide, over the half of the electrode closest to the input end of the CCD, so that the corresponding potential difference across the semiconductor is reduced and its potential minimum is not so deep [Ref. 7]. The stepped oxide approach in Figure 18 (a) accomplishes this by increasing the oxide thickness, while the diffused

implant approach in Figure 18 (b) uses a more highly doped semiconductor material of the same polarity as the substrate to reduce the depletion layer thickness.

The two-phase system is attractive for the following reasons: it allows a relatively simple clock design; it allows a relatively simple layout of interconnections on the semiconductor chip; possible higher packing densities; and charge transfer can be faster because there is less danger of charge spillage due to the asymmetric potential wells. However, two-phase systems also have disadvantages such as smaller charge handling capability than comparable three-phase devices. Additionally, two-phase systems require more specialized design and fabrication technology than three-phase systems; Magic does not allow the design of stepped oxide structures or diffused implants. Therefore, a two-phase system design is not possible for this project with our currently available tools.

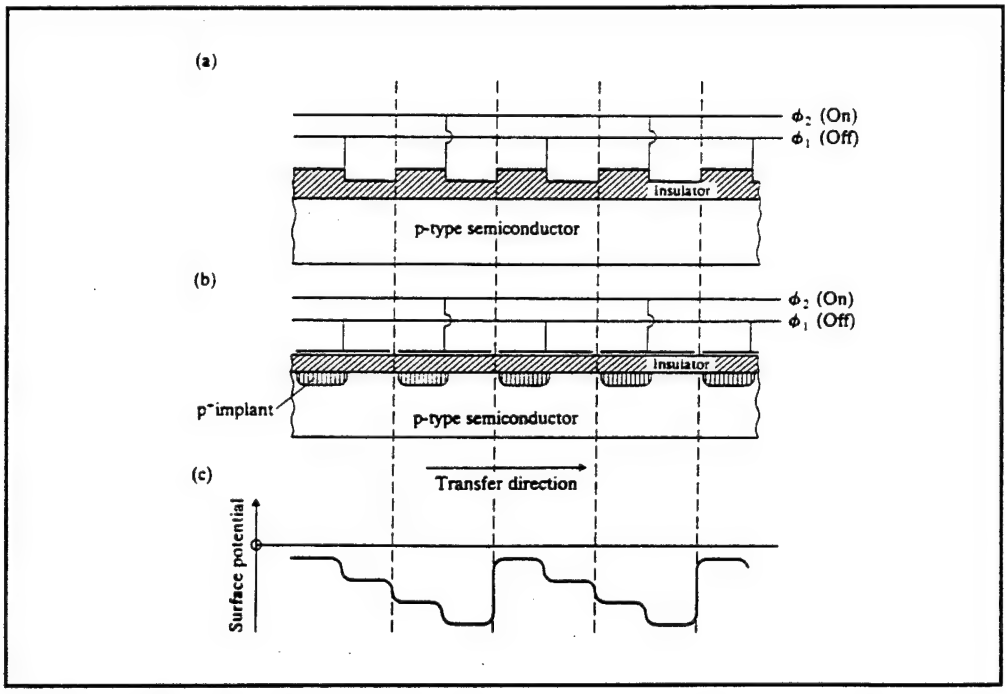

Figure 18. Two-Phase Clock Structures: (a) stepped oxide; (b) diffused implant. From Ref. [7].

c. One-Phase Systems

Any two-phase system can be operated as a one-phase system if one set of electrodes is connected to a fixed bias and the other set is pulsed positive and negative

with respect to this fixed level. While one-phase systems are attractive from an operating standpoint, numerous processing steps are required, and tight tolerances must be kept on ion implants and on CMOS processing and electrode location. Furthermore, the signal handling capacity of one-phase systems is low relative to other clocking systems. A one-phase CCD design in not possible with the tools and processes available at NPS.

d. Four-Phase Systems

A four-phase system, as shown in Figure 19, removes some of the practical problems of the three-phase system while keeping the electrodes as simple as possible. A device with four electrodes per cell can be operated as either a two-phase device with electrodes grouped in pairs and means provided for obtaining the necessary potential well asymmetry (as discussed above) or a four-phase device. Operating as a four-phase device, this system can use one of two different clocking schemes which are shown in Figure 20. The first clocking scheme, in Figure 20 (a), is similar to the three-phase clocking. In the second clocking scheme, in Figure 20 (b), each succeeding clock pulse is shifted one quarter of a clock period to the right, which results in ϕ_3 and ϕ_4 being the inverses of ϕ_1 and ϕ_2 respectively. The charge storage capability of the second clocking scheme is approximately double that of the first, and the fall time requirement of the clocks is somewhat relaxed. For these reasons, the four-phase system with the second clocking scheme as shown in Figure 20 (b) was chosen as the system of choice for this project. The procedure for designing the four-phase on-chip clocking circuit used for this project is detailed in Appendix A.

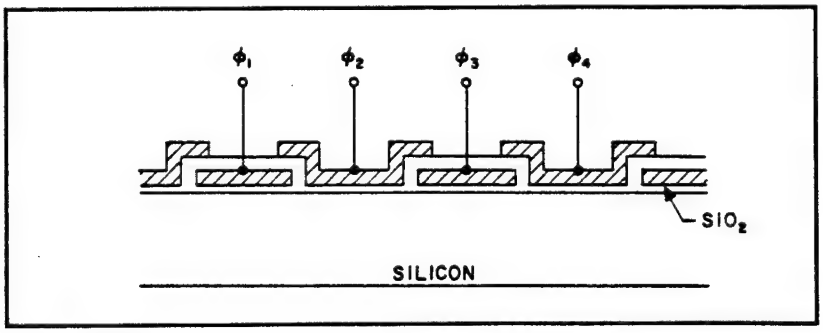

Figure 19. Four-Phase Clock Structure. From Ref. [3].

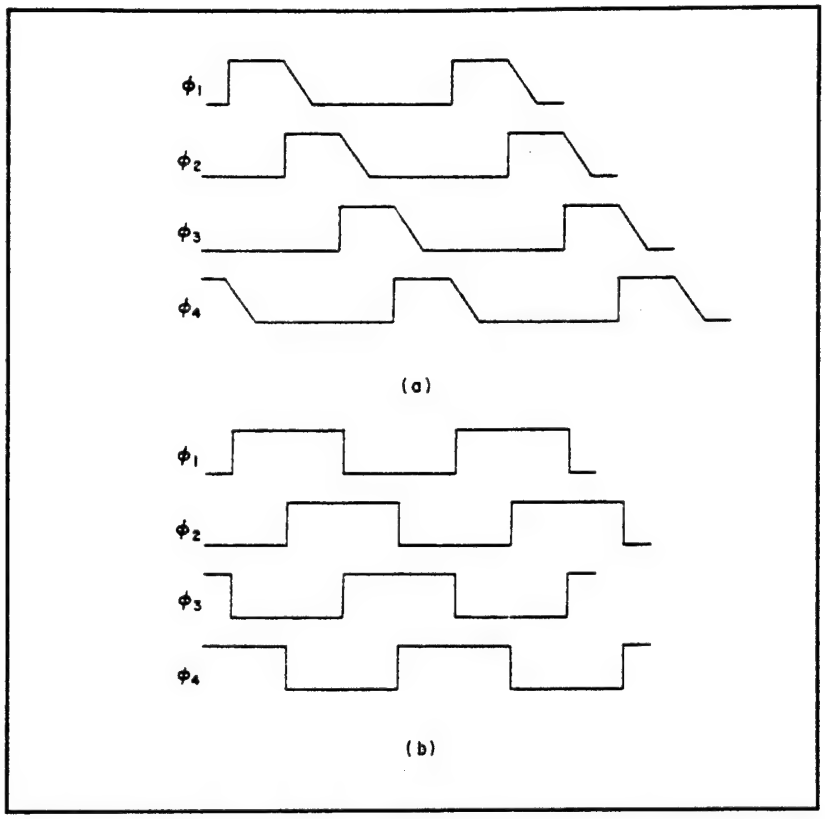

Figure 20. Clocking Schemes for Four-Phase System. From Ref. [3].

5. Electrode Cell Size

The electrode gate length is generally made as narrow as possible in order to minimize the carrier transit time. CCDs with electrode gate lengths as small as 4 μm [Ref. 10] to over 12 μm have been designed. With smaller gate lengths, the CCD will have higher speed capabilities, a lower capacitive load, and a smaller charge handling capacity. Larger gate lengths can transport more charge but have a higher capacitive load and cannot operate at higher frequencies. With the aim of this project to design and gain a better understanding of a working CCD, a conservative gate length of 8 μm with 2 μm overlaps was chosen. Therefore, the total cell length for the proposed BCCD is 26 μm. The die size available was 2.24 mm with about 20% required for bonding pads, making 1.79 mm available for the CCD length; this allowed the design of a 64-stage CCD.

In a four-phase CCD, which was chosen for this project, the charge packet is stored

under two adjacent electrodes as it is transferred along the channel. If the gate voltages are driven by clocked square waves, the full storage capacity of the two gates should be available. However, at higher frequencies, sinusoidal gate voltages are more common. In this situation, adjacent gates are 90° out of phase and hence cannot offer the full storage capacity of two adjacent gates. The minimum total storage capacity occurs when two adjacent gate voltages are equal and changing in opposite directions. At this point, the storage capacity of each cell is $\sqrt{2}$ / 2 or 70 percent of maximum [Ref. 11].

Work done by French and McNutt determined that the charge storage requirement must be at least 1.5×10^6 charges per cell [Ref. 11]. Since it was determined that about 70 percent of the two gate storage capacity is available under worst case conditions, the effective width of two consecutive gates is (0.7 x 2 x 8 μm) - 2 μm = 9.2 μm. The charge capacity of this type of CCD was calculated to be about 8×10^{11} / cm^2 [Ref. 11]. Therefore, the cell width must be at least 20 μm. The actual cell width was kept at this value to keep the capacitive load of the clock and its output drivers manageable. This cell width is also reasonable in terms of the space that must be available for input and output circuits at the channel ends.

B. ELECTRICAL INPUT TECHNIQUES

As has been discussed earlier, information in CCDs is transmitted and processed in the form of packets of signal charge. To be useful, the charge packets must be generated in such a manner as to have some functional relationship with the input signal. In digital systems, the input structures can be quite simple since any charge greater than a set quantity is generally considered a 'one' and less charge is considered a 'zero'. However, for an analog circuit, the input method must be more exact in order to retain all the information, yet not introduce noise or decrease the signal-to-noise ratio. Additionally, a linear relationship between the input voltage and the size of the charge packet is desirable for

simplicity. An expression that relates charge packet size to surface potential, ϕ_S, and the electrode voltage, V_G, is

$$Q_{SIG} = C_{OX}\left(V_G - \phi_S - \sqrt{2V_O\phi_S} \right) \qquad (7)$$

where V_O is a constant given by $(qN_A\varepsilon_S)/(C^2_{OX})$ and

q is the magnitude of the charge

N_A is the acceptor atom doping level

ε_S is the permittivity of silicon

Q_{SIG} is the charge packet size.

This equation will help to refer the quantities which determine ϕ_S and Q_{SIG}; this equation will be referred to in the following subsections.

1. Single Control Gate Input Techniques

Various methods have been developed to obtain a linear input. One input arrangement which has been used contains an input diode, one input transfer or control gate, and one storage electrode from the CCD body, as shown in Figure 21. The input diode consists an n^+ diffusion region in the p-type substrate which acts as a source of electrons for the channel. The input gate controls the charge flow from the input diode to the potential well under the storage electrode.

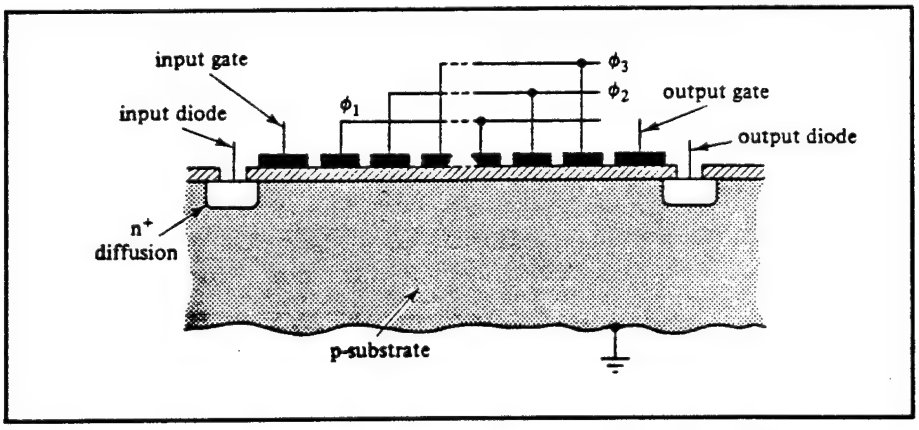

Figure 21. Simple CCD Input Structure. From Ref. [6].

a. Dynamic Current Injection

Referring to Figure 21, the input diode, the input gate, and the potential well formed under the first CCD body electrode can be regarded as an MOS transistor. However, now the 'drain' region of the device is a potential well rather than a diffusion. In this technique, the input gate is kept at a constant potential, and the input signal is connected to the input diode, as shown if Figure 22. This results in the magnitude of the charge packet depending on the injection time and on the input diode-to-input gate voltage, similar to a MOS transistor where the drain current is modulated by the gate-to-source voltage. Operating in saturation, the input device conducts for 1/p of the clock period, T_C, where p is the number of phases. The injected signal, Q_{SIG}, is then given by

$$Q_{SIG} = I_{D\ SAT}\, T_C / p \qquad (8)$$

where $I_{D\ SAT}$ is a non-linear function of the input diode-to-gate voltage.

There are two significant disadvantages of this dynamic current injection input technique. First, the amount of charge injected depends on the clock period, so any

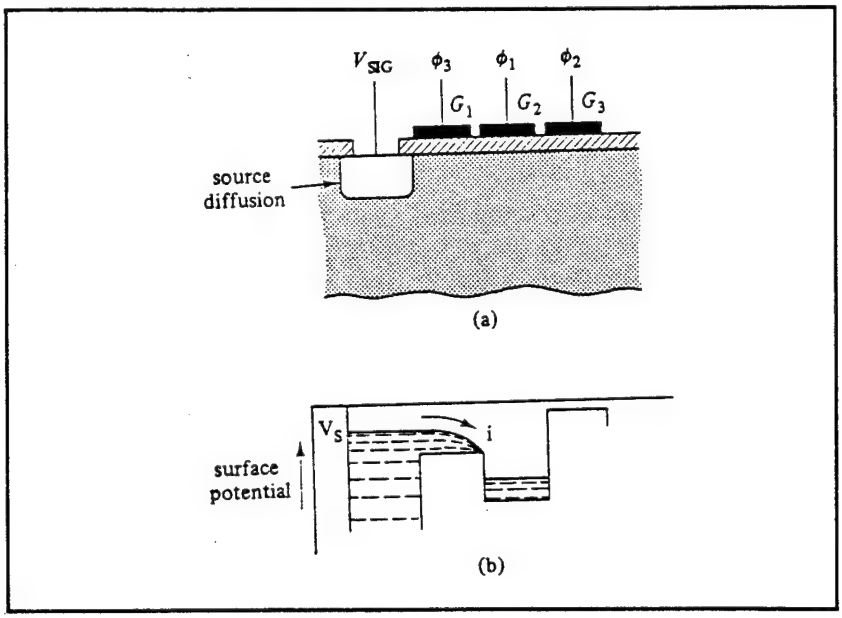

Figure 22. Charge Injection Input Circuit: (a) connections; (b) operation. From Ref. [6].

variation in T_C causes an error in Q_{SIG}, as can be seen from equation 8. Second, for much of the operating range of an MOS transistor, the drain current is approximately proportional to the square of the gate-to-source voltage, which is clearly nonlinear. Therefore, in the CCD application, Q_{SIG} will be a non-linear function of the input diode-to-gate (signal) voltage.

b. Diode Cut-Off

Referring to Figure 23, a pulse is applied to the input gate G_1 while the signal is applied to the input diode. Looking at the input diode, the input gate, and the potential well under the first CCD body electrode as a MOS transistor, as above, G_1 can be pulsed sufficiently hard to cause the transistor to operate in the non-saturated mode. This will cause the surface potential under G_1 and G_2 to be set to the potential of the input diode as in Figure 23 (b). Switching input gate G_1 off while G_2 remains on causes the charge under the input gate to flow back to the source, isolating the charge under G_2 from the input diode diffusion. Therefore, this technique sets the potential under G_2 to the voltage of the input signal.

From equation 7, the magnitude of the charge packet is not linearly dependent of the input voltage. But, a more significant disadvantage of this input technique is that when the input gate G_1 is turned off, the charge under it divides between the input diode and the first CCD electrode well, causing an error in the quantity of charge injected. The effects of charge partitioning can be lessened by making the input gate electrodes smaller than the transfer electrodes, which reduces the impact of the charge that is spilled 'forward'.

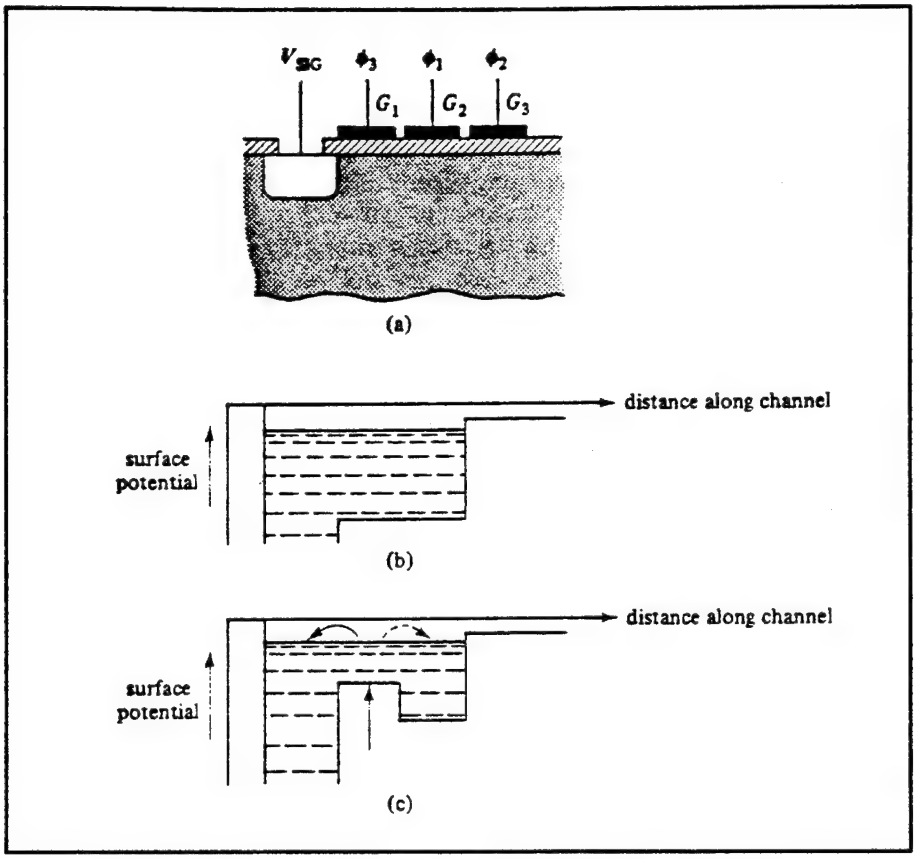

Figure 23. Diode Cut-Off Technique. From Ref. [6].

2. Multiple Control Gate Input Techniques

The above input techniques have only one input or control gate. Therefore, the input diode is adjacent to a clocked electrode, which allows clock pulse noise to feed through and on to the charge packets. An easy way to eliminate this clock pulse noise is to add a second or more gate electrode to the input structure.

a. Potential Equilibration Input Technique

The potential equilibration input (also called the 'fill-and-spill') technique provides a linear input method. Here, the gate adjacent to the input diode, G_1, is held at a fixed potential, while the input signal is applied to the second electrode, as shown in Figure 24. The surface potential under the input diode is brought to a very low potential by

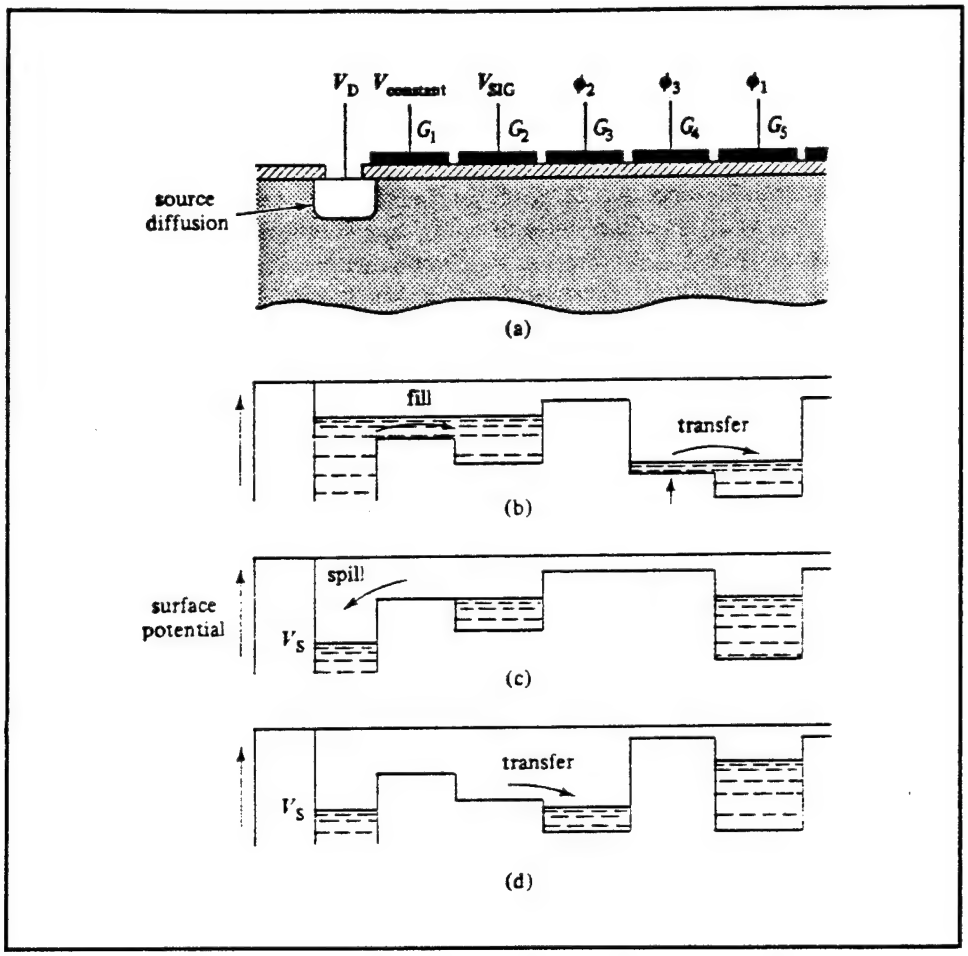

Figure 24. Potential Equilibration Input Technique: (a) input gate structure; (b) and (c) potential profiles showing fill and spill operations; (d) potential profile showing transfer of input charge signal from input well to CCD register. From Ref. [6].

reducing the input diode applied voltage for a short time, which causes the storage well under G_2 to fill with charge. The surface potential under the input diode is then returned to its high potential, causing the excess charge from the storage well to spill back into the diode region. The size of the charge packet in the well beneath G_2 is given by equation 7, in which V_G is represented by the signal voltage V_{G2}; ϕ_S is represented by V_{G1}, and is held constant; and Q_{SIG} which varies linearly with the input voltage signal. The potential equilibration input technique adds very little noise to the signal, provided an adequate

period of time is allowed for charge equilibration to take place. Additionally, forward spilling of charge does not occur with this technique. The problem with this input mode, however, is the length of the equilibration time can limit the device sampling frequency, hence the speed of the CCD [Ref 11].

b. Pulsed Diffusion Input

In the pulsed diffusion mode, shown in Figure 25, the input signal is applied directly to the input diffusion of the CCD. The input control gates G_1 and G_2 are biased in the charge accepting mode so as not to inhibit the flow of carriers injected from the diffusion. The charge injected into the input well under gates G_1 and G_2 is proportional to the voltage applied to the CCD input diffusion, represented by arrow (1). When the potential under the first CCD body gate electrode, ϕ_1, is lowered (2), the charge flows into the CCD (3) to form a charge packet. The amount of charge injected into the CCD register depends on the input voltage, the length of the input well, and the time gate ϕ_1 is in a low potential or non-blocking condition. It has been found that this technique is continually in a transient operating mode and never reaches equilibrium during the charge injection cycle. Therefore, the lack of potential equilibrium precludes a linear relationship between the amount of charge injected into the CCD register and the input voltage. This injection technique is most suitable for injecting digital signals into CCDs, but not analog signals as this project requires. Experimentation has shown that charges can be injected into a CCD with this input configuration at speeds of up to 200 MHz [Ref. 11]. Another disadvantage of this technique is the large noise associated with it.

c. Charge Partition Mode

In the charge partition mode, a charge packet is formed in the potential under gates G_1, G_2, and G_3 by biasing the input diffusion to inject charge and lowering the G_2 potential (1), as shown in Figure 26. This allows the carriers to fill the potential under the three control gates (2). The amount of charge present is proportional to the analog voltage signal on the input diffusion and the area of the potential holding well. After the charge equilibrates in the potential holding well, G_2 is quickly raised to split the charge

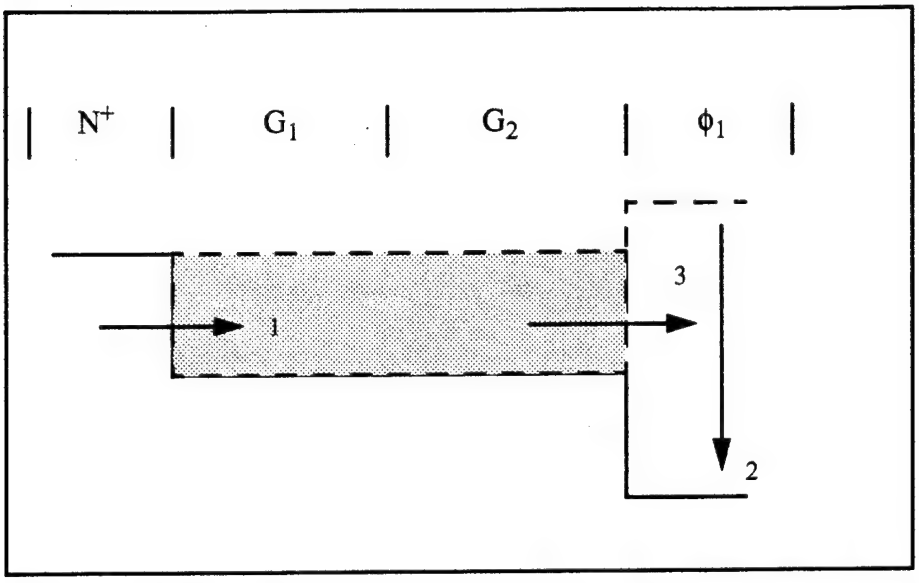

Figure 25. Pulsed Diffusion Input Technique. Modified from Ref. [11].

pool into two parts (3). The ϕ_1 potential clocks low (4), allowing the charge packet under G_3 to transfer into the CCD register (5). The difference between the potential on the N^+ diffusion and on the G_3 potential determines the size of the charge packet; therefore, the input signal can be applied to either of these contacts.

The charge partition input can be operated at very high speed, up to 500 MHz [Ref. 11]. This high speed is possible because both the flow of charge from the forward-biased N^+ diffusion and the partition of the charge packet by the G_2 gate are fast field-aided processes. However, this technique is subject to large partition noise.

C. CHARGE SENSING TECHNIQUES

Once information, in the form of charge packets, has been injected into the CCD, it is transferred along the channel under the control of the clock voltages on the electrode gates. To be useful, these charge packets must be detected or read out at some point. If the detection is to occur at the end of a CCD delay line, then the detection technique can be destructive to the signal because it has to be removed at the end of the CCD register

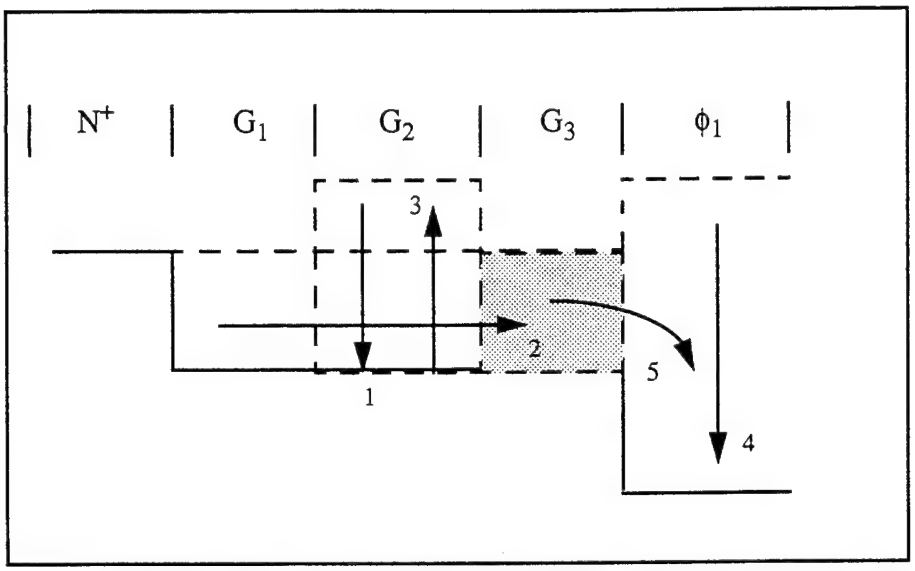

Figure 26. Charge Partition Input Technique. From Ref. [11].

anyway. However, in a multi-tap situation where the signal must be sensed multiple times as it propagates through the CCD, the detection technique must be non-destructive. Another consideration is whether a current or voltage output is required from the detection circuitry. Both of these issues effect the choice of the detection method and have lead to the development of various sensing circuits. This subsection examines several different methods for signal charge sensing and the optimum choice for the BCCD design of this project.

1. Direct Output

The simplest output method obtainable from a CCD is the direct output technique. With this method, the signal charge is removed from the output diffusion directly and is measured by determining the voltage drop across a fixed resistor. The problem, however, is that the output signal voltage is often very small to make this method practical.

2. Floating Gate Output

The floating gate technique has been used in CCD signal processors to nondestructively detect the charge packet in a specific cell by sensing a change in the surface channel capacitively. In this technique, a 'floating gate' is located above the channel and beneath a

CCD electrode, which is biased instead of clocked as shown in Figure 27 (a). When a charge packet transfers under the 'floating gate' it produces, by capacitive coupling, a change in the potential in the floating gate. This change in potential is then sensed by an on-chip MOS transistor. An example of this output structure is shown in Figure 27 (b). From this technique the following equation applies for an SCCD:

$$\Delta V_{FG} \approx Q_{SIG} / C_P, \qquad (9)$$

where $C_P = C_{OX2} + C_G$

ΔV_{FG} is the change in voltage

Q_{SIG} is the injected signal charge

C_{OX} is the capacitance between the floating-gate and the overlying CCD electrode

C_G is the input capacitance of the MOS sense transistor.

This approximation is not valid for BCCDs because the channel is much further away from the surface, hence the capacitive coupling between the charge and the floating gate is much smaller. This type of detection method is desirable for SCCDs with good linearity. A disadvantage of the floating-gate sense technique is that to obtain high sensitivities, C_P in equation 9 must be small. One way in which C_P can be reduced is by increasing the oxide thickness above the floating gate which reduces C_{OX2}. However, this implies that the bias voltage must be set high, possibly above the usual supply voltage. Additionally, a thick oxide layer is not available as a design parameter using the Magic layout editor and the MOSIS process.

3. Floating Diffusion Output

Floating output diffusion sensing is the most widely used scheme for detecting the output charge at the end of a CCD. Referring to Figure 28, this output structure consists of an output gate (OG); a MOS transistor structure consisting of a floating diffusion (FD), a reset gate, and a voltage source diffusion; and an amplifier circuit which monitors changes in the floating diffusion voltage. In normal operation, the voltage on the reset gate is intially driven high ($V_{R,hi}$) so that the channel potential is greater than V_{DD} ($\phi_{R,hi} > V_{DD}$). Therefore, the floating diffusion potential is reset to V_{DD}. After the voltage

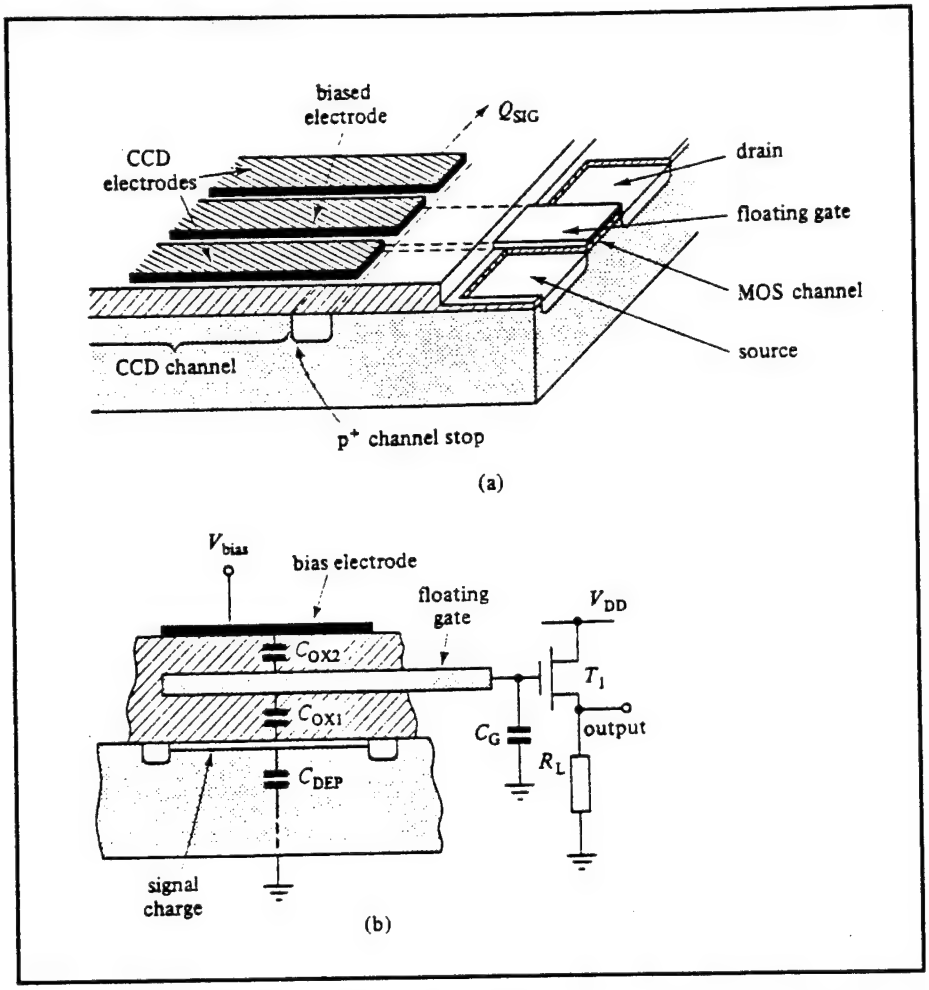

Figure 27. Floating-Gate Sensing Technique: (a) general scheme; (b) basic model with sense transistor. From Ref. [6].

on the reset gate is returned low ($V_{R,lo}$) with the channel potential falling to $\phi_{R,lo}$, the floating diffusion becomes disconnected from the voltage source V_{DD}. The floating diffusion remains at V_{DD} immediately after the voltage on the reset gate is returned low.

Next, a signal charge packet is dumped onto the floating diffusion from the CCD channel, causing a change in the floating diffusion voltage V_{FD}. An expression relating this is

$$\Delta V_{FD} = Q_{SIG} / C_{FD} \qquad (10)$$

where ΔV_{FD} is the change in voltage

Q_{SIG} is the injected signal charge

C_{FD} is the total capacitance at the floating-gate diffusion node.

Output gate OG is held at constant voltage during both the reset operation and the charge dump to prevent clock coupling noise from the CCD register to the floating diffusion.

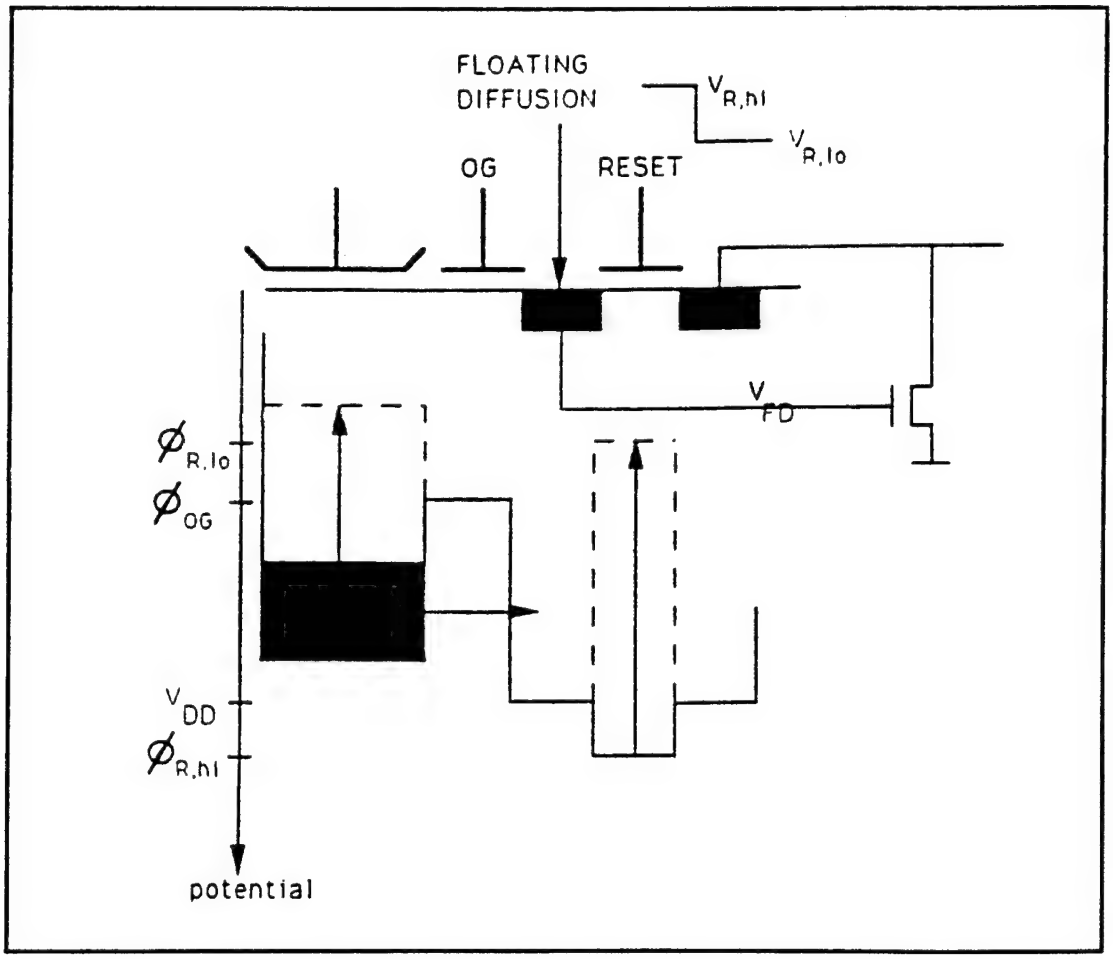

Figure 28. Floating Diffusion Output Structure. Modified from Ref. [5].

A potential downside of this output circuit is that C_{FD} is made up of mostly nonlinear capacitance. However, in most cases, other stages introduce more nonlinearity than is introduced here. The magnitude of C_{FD} can be reduced by precharging the floating diffusion to a large voltage relative to ΔV_{FD} ($V_{DD} \approx 10v$), which has the effect of linearizing ΔV_{FD}.

After each charge packet has been detected, the reset gate is pulsed high to reset the floating diffusion potential, prior to the arrival of the next charge packet.

4. Distributed Floating-Gate Amplifier

The floating gate output method, described above, allows the same charge packet to be sensed multiple times as it transfers along the channel because this method is non-destructive. If the amplified signals from many floating gates are combined with the correct time relation, the overall sensitivity increases linearly with the number stages, N, while the signal-to-noise ratio can be improved by as much as $\sqrt{N}$ [Ref. 6]. This principle is the basis of the Distributed Floating-Gate Amplifier (DFGA). Looking at Figure 29, the outputs from each stage are combined in a second, larger CCD. Each floating gate in the primary CCD register acts as the input in a current injection method, feeding successive charge packets into the output CCD. This output method has demonstrated the highest charge detectability of all output methods. However, it is very sensitive to dc variations in the floating gate potentials, and is therefore very difficult to operate in a stable manner [Ref. 5].

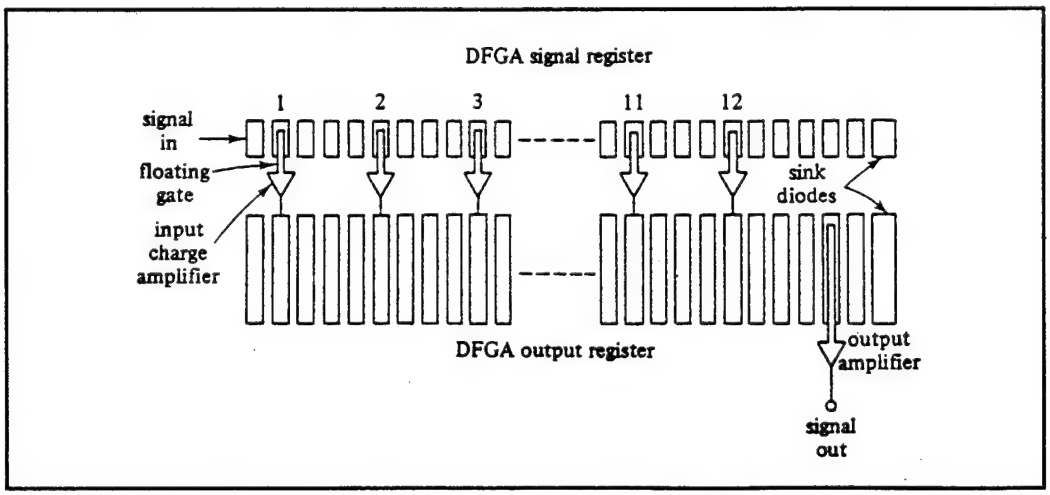

Figure 29. Distributed Floating Gate Amplifier Organization. From Ref. [6].

D. PERIPHERIAL CIRCUITS TO THE CCD

So far, this chapter has examined design decision about the CCD register itself. But, other peripheral circuits are needed in order for the CCD analog delay line to work. These circuits are the on-chip clock generator, the clock drivers, and the output amplifier.

1. Clock Circuit

As was discussed earlier in this chapter, a four-phase clocking scheme was selected for the operation of the CCD analog delay line. The clock circuit not only propagates the signal charge along the CCD channel, but also synchronizes the input of charge into the CCD register body and the detection of that charge at the end of the register. Because the clock is central to the operation of the CCD, it was designed and placed directly on the chip adjacent to the CCD. The design began with a desired state diagram of the clock's behavior and culminated with a logical simulation of the extracted design layout using ESIM. The details for the clock design are given in Appendix A.

2. Clock Output Driver

Each stage of the analog delay line has four electrode gates associated with it. Each gate electrode in a stage has a counterpart in each of the other 63 stages to which it is electrically connected. Therefore, all of the first gates are electrically connected together, all of the second gates are connected together etc... This allows for a smooth transfer of charge down the CCD channel and for 64 signals to be in the channel at any one time. Each of the four phases of the clock circuit is responsible for driving one of these groups of electrode gates, which is a relatively large capacitive load. In order for the clock to adequately drive this large capacitive load, each of the clock signals must be passed through a chain of inverters to boost the signal. For the CCD analog delay line described here, each clock needs four output drivers. In this way, a single digital clock can drive the capacitive load of an entire CCD. The details for the clock output driver design are given in Appendix B.

3. Output Signal Amplifier Circuit

By the time the charge signal reaches the end of the CCD register channel, it will be weakened and degraded due to incomplete charge transfer inefficiencies and carrier

trapping state inefficiencies along the way. Although the use of a bulk channel reduces these effects, it does not entirely eliminate them. In order for the output signal to be useful, it must be sufficiently amplified after it has been detected. Therefore, an on-chip amplifier for boosting the output signal was designed and laid out at the output of the CCD. Fitting the requirements for low noise, high input impedance, and high gain, a differential amplifier was chosen as the type to design with. Details of the output signal amplifier circuit design are presented in Appendix C.

E. CCD DESIGN DECISION SUMMARY

1. CCD Register Structure

This subsection is to briefly summarize the design decisions regarding the CCD structure from the many options discussed. First is the issue of bulk-channel CCD versus surface channel CCD. Besides having a higher transfer efficiency and higher transfer speeds, BCCDs are the only CCD type that MOSIS design rules allow, thereby making the decision for us. The next issue is the type of electrode gate material. The single metal gate, conductive channel, and polysilicon-aluminum gate designs are all relatively old technology designs with significant disadvantages to each. The double- and triple- polysilicon gate structures offer significant advantages, with the triple-polysilicon structure having the minimum failures due to shorts between gates and the smallest desirable gate size. However, the triple-polysilicon technology is not accommodated by the MOSIS process; hence we must use the double-polysilicon gate structure.

On the issue of channel confinement, the diffused channel stop method is the most suitable; it is relatively easy to design into the CCD with Magic's pdiffusionstop material. Magic does not allow one to design with thick field oxide, thereby ruling out the thick field oxide method. Additionally, the electrostatic field shield method is too complex and high-risk, with each part of the field shield required to be connected to a bias voltage.

With regards to clock phases, one- and two- phase systems are not possible with the currently available tools because these tools do not allow stepped oxide structures, diffused implants, or the gradient doping necessary to establish asymmetry within the CCD

cells. While three-phase systems are definitely possible with our available tools, a three-phase clock is awkward to implement. A four-phase system which has the third and fourth phases as the complements of the first and second phases respectively, has a large charge storage capability and is not too difficult to implement; thus was the choice for the clocking decision.

The electrode gate size is 8 μm in length with 2 μm overlap, which will allow a CCD with 64 stages to fit in the allowed die size length. The CCDs bulk channel width will be 20 μm.

2. Multiple Designs on One Chip

By its nature, the CCD delay line is much longer than it is wide. This leaves a great deal of unused area on the die. To utilize this area, four different CCD analog delay line designs have been design and laid onto the chip using Magic. Two of the designs will implement the single gate dynamic current injection technique, as it is a relatively simple design. Of these two CCD designs, one will have the pdiffusionstop material for lateral charge confinement and one will not. The other two CCD analog delay lines will implement the three-gate charge partition mode injection technique. This technique offers the most advantages of the three multi-gate input techniques examined. As before, one of these designs will have the pdiffusionstop material for lateral charge confinement and the other will not.

All of the four analog CCD delay lines will use the floating diffusion output technique for signal charge detection. Additionally, each CCD will have its own clocking circuit with the four accompanying drivers. Each delay line will use its own output amplifier, based on the same differential amplifier design, at the output end of the CCD delay line.

IV. CMOS LAYOUT

Once the CCD delay lines and the periphery circuits were defined, the layout of these circuits was accomplished using Magic. Design rules for the 2 μm CMOS N-well technology were used to verify correct layout of the circuits. A discussion of the layout procedures for CCDs is given, followed by Magic layouts of the CCD analog delay line structures and overall chip. The Magic layouts for the on-chip clock, clock output driver, and differential amplifier are presented in Appendices A, B and C, respectively.

A. LAYOUT OF CCDs WITH MAGIC

Using the latest MOSIS Magic technology file, a bulk-channel CCD device in Orbit's process is implemented or laid out by the use of the following layers:

bccdiffusion (bd) for the implant layer
nbccdiffusion (nbd) for the active terminal layers
nbccdiffcontact (nbdc) for the active terminal layers

The use of these layers to layout a BCCD is illustrated in Figure 30. The 'nbdc' layer is the corresponding contact tile for the 'nbd' layer. All of the layers are necessary in order to make the BCCD device work. The 'bd' layer is used to show where the buried channel is located under both of the polysilicon layers while the 'nbd' and 'nbdc' are used for the terminal connections at the active layer for signal input and output. A DRC error will appear around the 'bd' layer when laying out the CCD. MOSIS representatives have stated to ignore this DRC error, as MOSIS chooses to enforce the overlap of the layers such as poly and poly2 to form a normal bulk-channel CCD device. The two active layers and the single 'bd' well layer at the bottom of Figure 30 are shown for better illustration.

Figures 31 through 34 show the Magic layouts for the four different input structures of the four CCD delay lines on the chip. Figure 35 shows the Magic layout of the floating diffusion output structure that is common on all four of the CCD delay lines. Figure 36 shows the overall chip floor plan for the four CCD delay lines. Figure 37 shows the Magic layout of the entire chip.

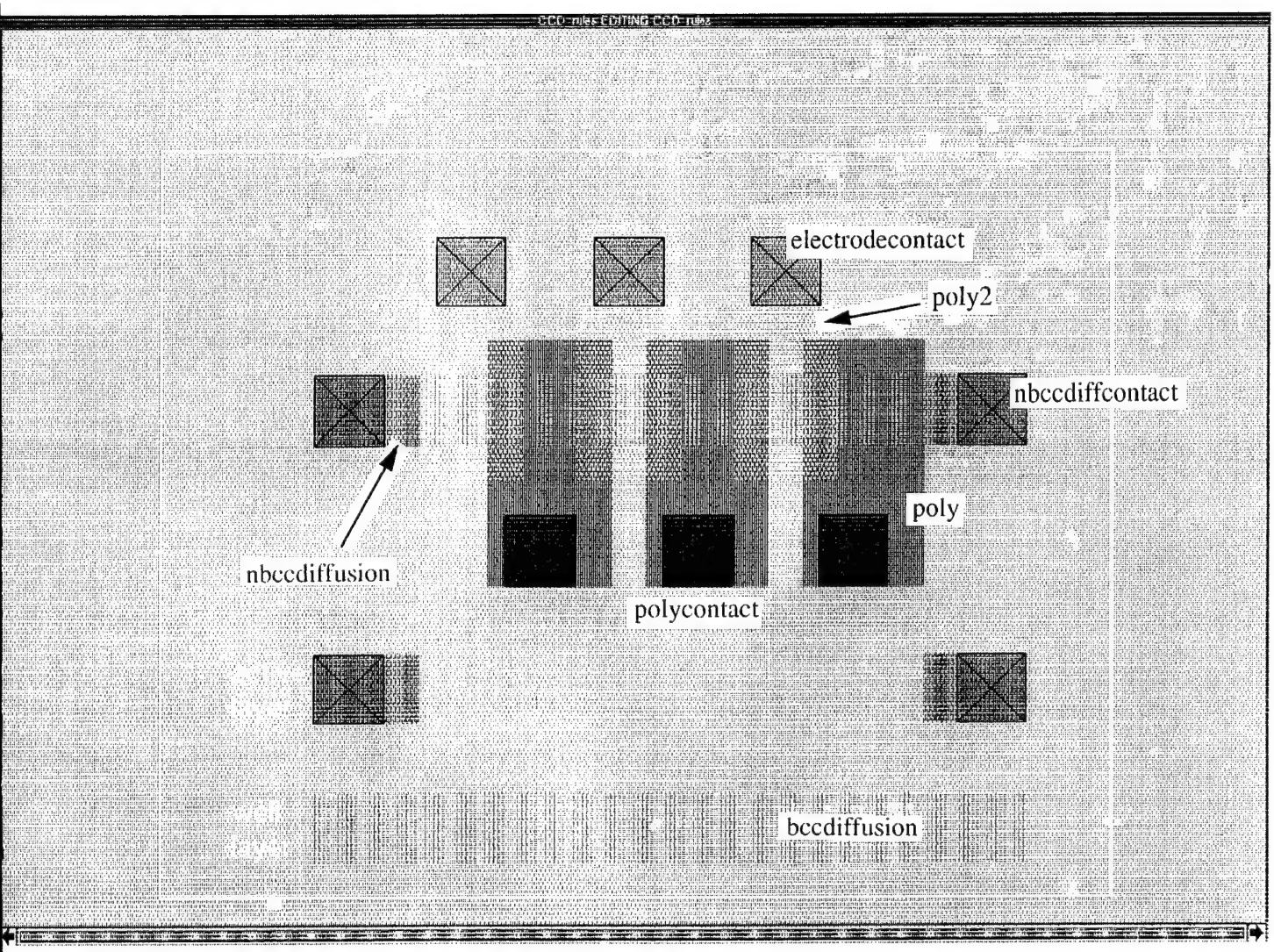

Figure 30. Magic Layout of a Buried-Channel Charge-Coupled Device.

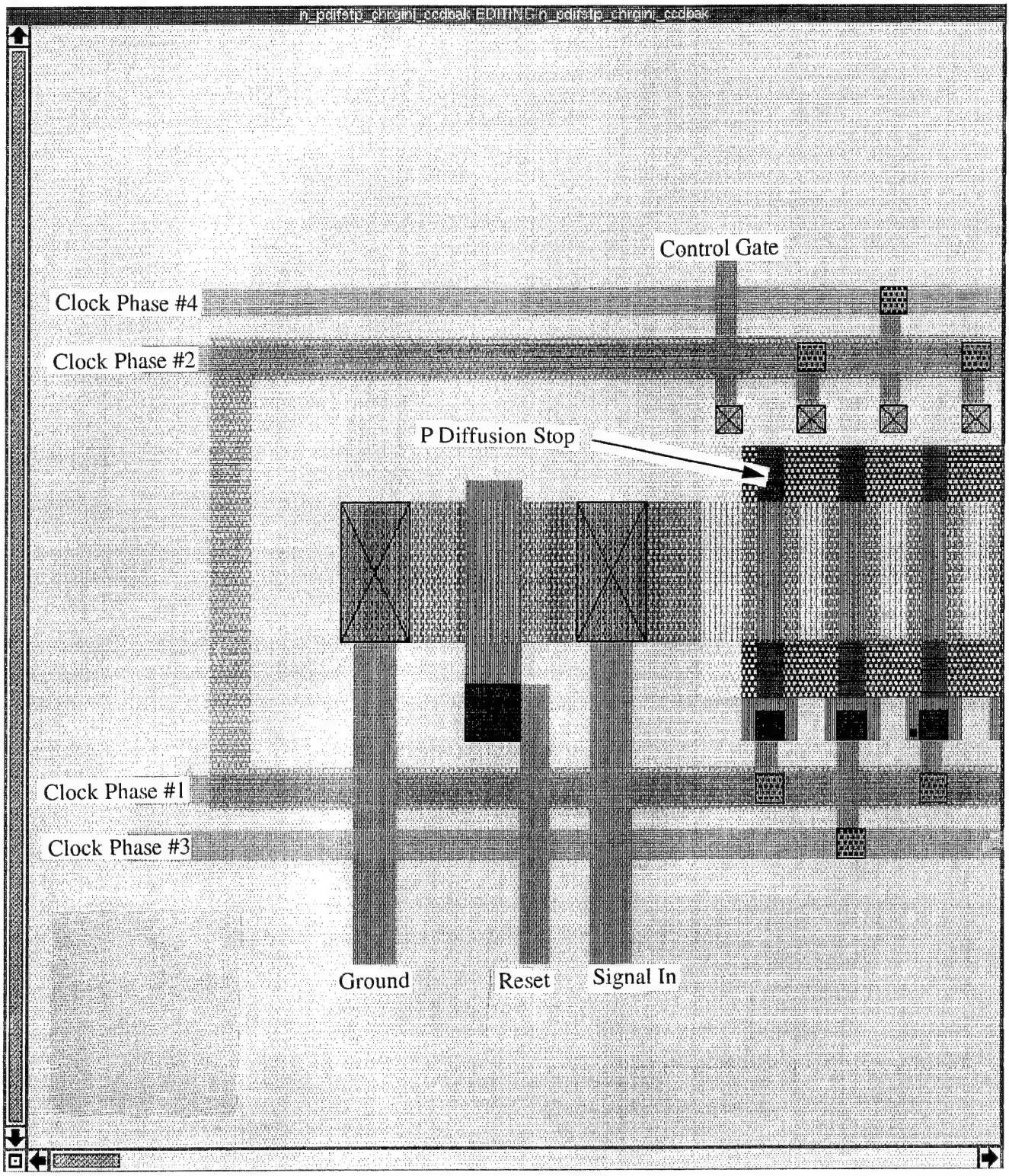

Figure 31. BCCD Delay Line Charge Injection Input Structure (with P Diffusion Stop).

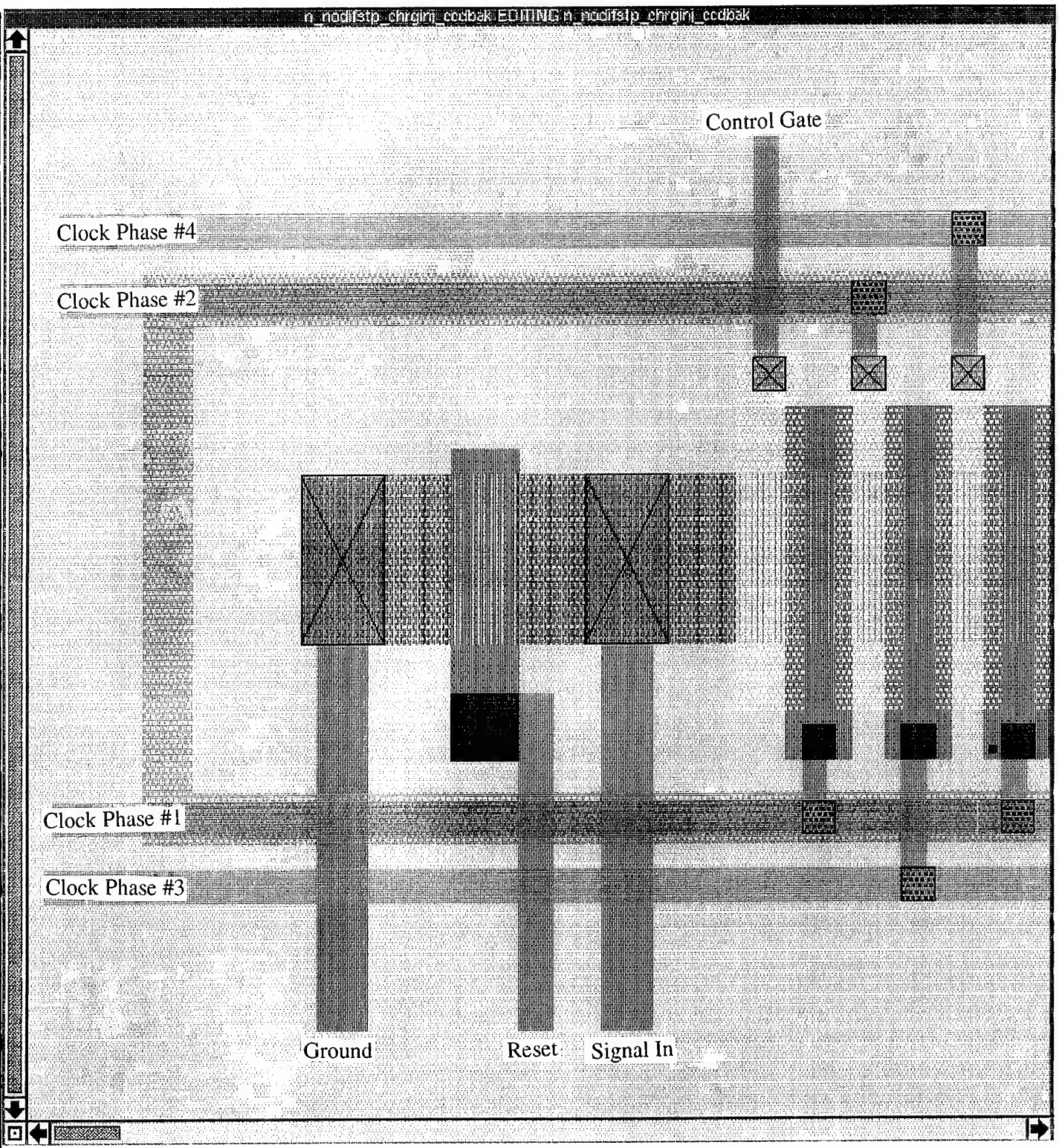

Figure 32. BCCD Delay Line Charge Injection Input Structure (without P Diffusion Stop).

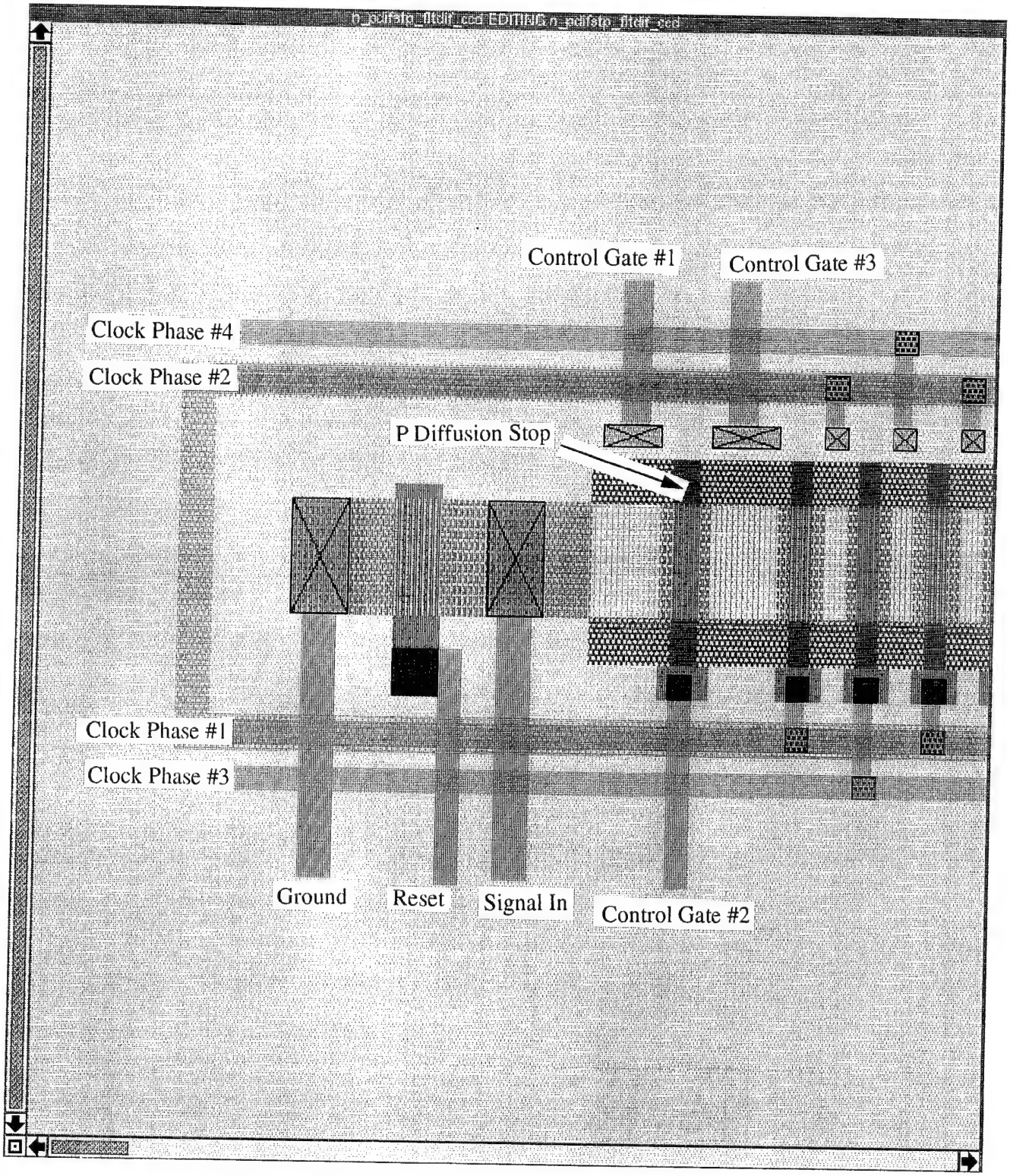

Figure 33. BCCD Delay Line Charge Partition Input Structure (with P Diffusion Stop).

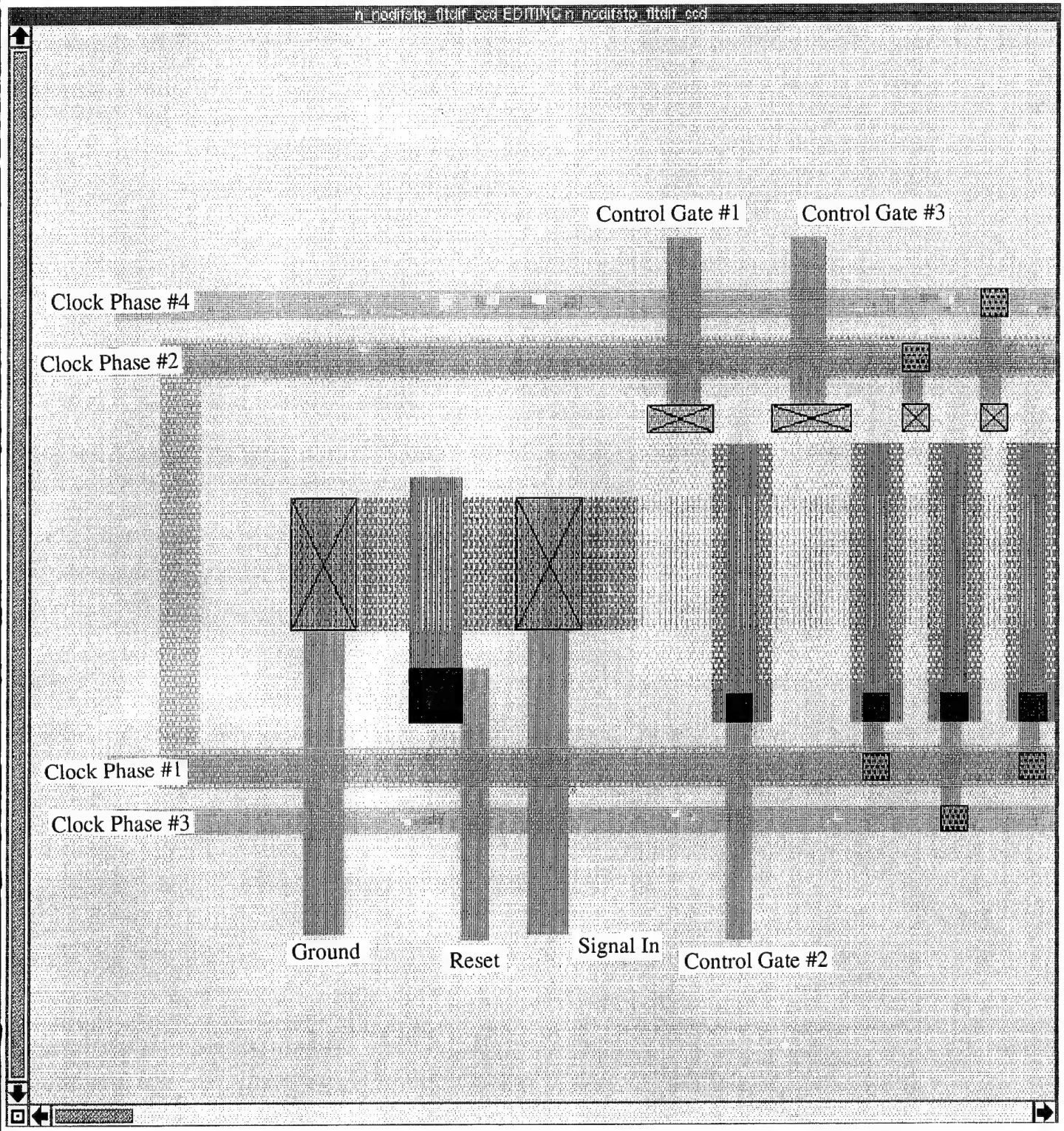

Figure 34. BCCD Delay Line Charge Partition Input Structure (without P Diffusion Stop).

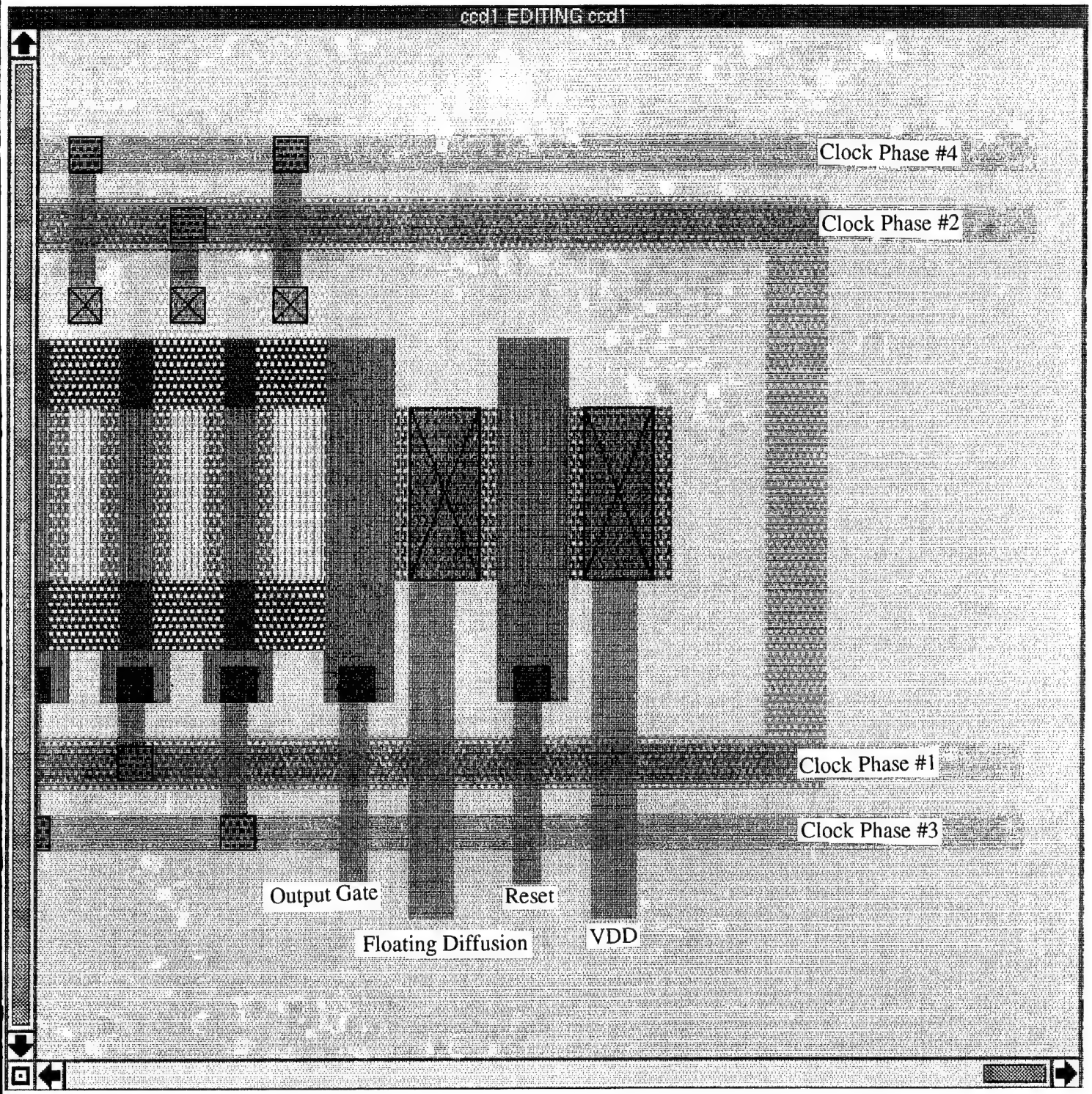

Figure 35. BCCD Delay Line Floating Diffusion Output Structure (with P Diffusion Stop).

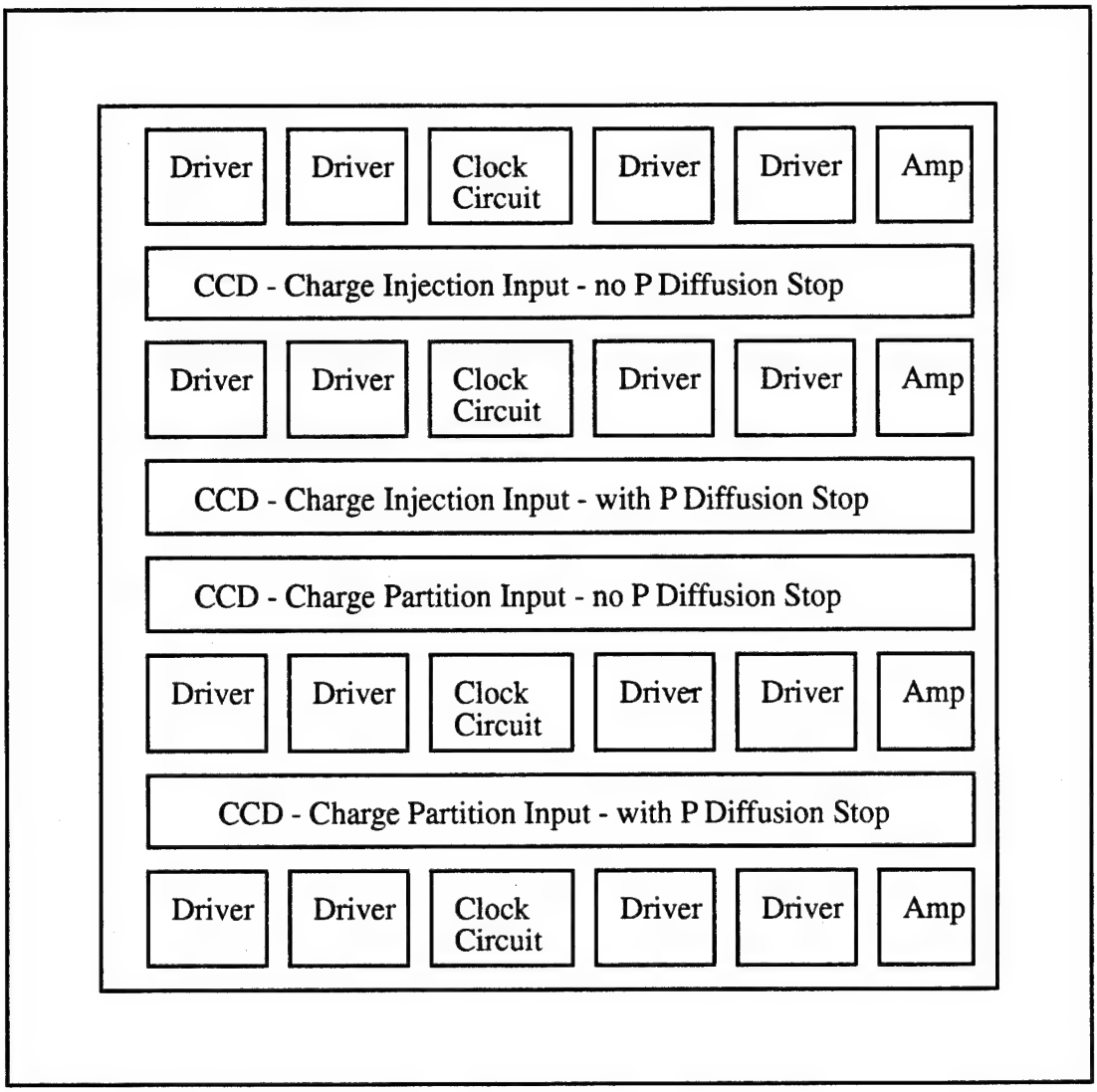

Figure 36. Chip Floor Plan.

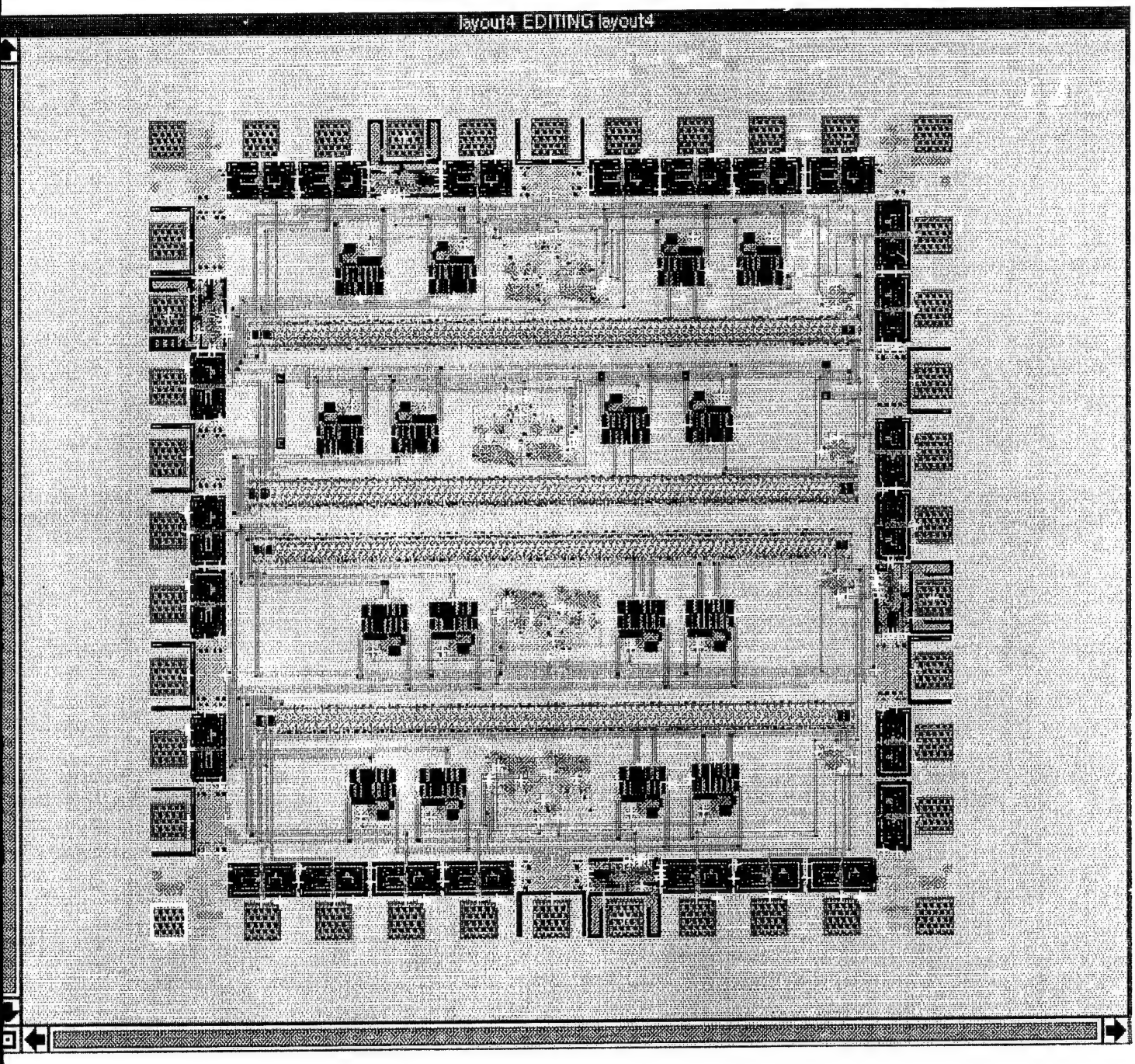

Figure 37. Magic Layout of Entire Chip.

V. CHIP TESTING PLAN

Once this chip with four different CCD analog delay lines is fabricated and returned from MOSIS, it will need to be evaluated. This chapter discusses a methodology on how the chip should be tested. There are two subsections which cover CCDs with the charge injection input structures and CCDs with the charge partition input structures.

A. TESTING OF CCDS WITH CHARGE INJECTION STRUCTURES

In determining how to set up the chip to test the CCD delay line with the charge injection input structures, one must first know what parts of the CCD are connected to bond pads. Such a list follows with number in parenthesis for an arbitrary pad number:

CCD Input Structure
- Ground (1)
- Reset (3)
- Signal In (4)
- Control Gate (5)

CCD Output Structure
- Output Gate (6)
- VDD (2)

Clock Circuit
- Clock In (7)
- X (8)
- VDD (2)
- Ground (1)

Driver
- VDD (2)
- Ground (1)

Amplifier
- VDD (2)
- Ground (1)
- Signal Out (9)
- Vref (10)

The parts listed above with the same arbitrary bond pad number are connected to the same bond pad. As one can see, each of the two charge injection CCD delay lines has

connections to 10 different bond pads on the chip. Next, we'll look at how each of these bond pads could be connected for testing of the chip.

1. Ground

The CCD input structure, clock circuit, driver, and amplifier all have connections to the *ground bond pad.* This pad should be connected to the common ground of the test setup.

2. VDD

The CCD output structure, amplifier, clock circuit, and driver all have connections to the *VDD bond pad.* This pad should be connected to a +5 volt power supply.

3. Reset

The reset connection on the input structure is the only item connected to the *reset bond pad.* The purpose of this connection is to clear the input structure of any residual charge before testing the chip. To reset the input structure the reset line must momentarily be driven high to +5 volts and then returned low. This will allow residual charge to flow out to the ground connection. Therefore, it would be preferable to have the connection to the reset bond pad set up to a manual switch arrangement, so that the input can be reset when desired.

4. Signal In

The 'signal in' connection on the input structure is the only item connected to the *signal in bond pad.* This connection is the conduit for input test signals to the CCD delay line. At least initially, it would be advantageous to have the 'signal in' set up similar to the reset connection with a manual switch. The output signal should be examined when the input signal is zero and compare that to the output signal when the input signal is +5 volts. The easiest way to do this is with a manual switch arrangement. After satisfactory results are obtained with this simple input scheme, different types of input signals can be applied to the input of the chip to determine the chips capabilities.

5. Input Control Gate

The 'control gate' connection on the input structure is the only item connected to the *input control gate bond pad.* The input control gate is located between the input

diffusion region and the first gate electrode of the CCD register. The input control gate is held at a constant voltage, which is less than that of the CCD gate electrodes, less than +5 volts. Input charge from the source diffusion region flows over the potential barrier formed by the input control gate, and into the potential well of the first gate electrode. The higher the voltage applied to the control gate, the lower the potential barrier for electrons to flow over from the source diffusion. Since there are no known rules or formulas to go by, it would probably be best to begin testing with the voltage on the input control gate set halfway, +2.5 volts. Adjust this voltage up and down to determine the effects on the output signal.

6. Output Control Gate

The 'control gate' connection on the output structure is the only item connected to the *output control gate bond pad.* The output control gate is located between the output floating diffusion and the last gate electrode of the CCD register. The output control gate is held at a constant voltage which is less than that of the CCD gate electrodes, less than +5 volts. Its function is to prevent clock coupling noise from the CCD register to the floating diffusion. Here again, it would probably be best to begin testing with the voltage on the input control gate set halfway, +2.5 volts. Adjust this voltage up and down to determine the effects on the output signal.

7. Clock In

The 'clock in' connection on the clock circuit is the only item connected to the *clock in bond pad.* This connection is the conduit for an external master clock signal to the four phase clocking circuit. The master clock signal should be a square wave with a conservative frequency of about 10 kHz. Once satisfactory results are achieved with this relatively low frequency, the master clock frequency can be increased and decreased to determine the operating capabilities of the delay line.

8. X Input

The 'X' connection on the clock circuit is the only item connected to the *X bond pad.* This input to the clock circuit is always asserted high or +5 volts. This connection could be made the same as VDD.

9. Signal Out

The 'signal out' connection on the differential amplifier is the only item connected to the *signal out bond pad.* This connection is the conduit for the amplified CCD output signal to detection test equipment. In this case the best piece of detection equipment would be a respectable oscilloscope. The detection frequency should be the same as that of the master clock.

10. Vref

The 'Vref' connection on the differential amplifier is the only item connected to the *Vref bond pad.* This connection is used to adjust the bias for the differential amplifier. The range for Vref was simulated to be between 1.5 volts to 2.2 volts. Lowering the Vref voltage shifts the high gain region of the amplifier to the left. Going lower than 1.5 volts on Vref turns the amplifier off. Start out with Vref about 1.75 volts, as was simulated in Appendix C.

11. P Diffusion Stop/ No P Diffusion Stop

On each chip, there are two CCD delay lines which have charge injection input structures. One of these delay lines has a P diffusion stop for lateral charge confinement and one does not. The two delay lines share all the same bond pads except for the 'signal in' and 'signal out'. Once satisfactory CCD operation is achieved, these two different CCD delay lines should be compared in testing.

B. TESTING OF CCDS WITH CHARGE PARTITION STRUCTURES

In determining how set up the chip to test the CCD delay line with the charge partition input structures, one must first know what parts of the CCD are connected to bond pads. Such a list follows with number in parenthesis for an arbitrary pad number:

CCD Input Structure	
- Ground	(1)
- Reset	(3)
- Signal In	(4)
- Control Gate #1	(5)
- Control Gate #3	(5)

CCD Output Structure
- Output Gate (6)
- VDD (2)

Clock Circuit
- Clock In (7)
- X (8)
- VDD (2)
- Ground (1)

Driver
- VDD (2)
- Ground (1)

Amplifier
- VDD (2)
- Ground (1)
- Signal Out (9)
- Vref (10)

It turns out that the only difference between this listing and that of subsection A above is for bond pad #5 , the control gate. So with the exception of the control gate, everything for the test setup of the charge partition control input CCDs is the same as in subsection A above. For the sake of brevity, only the control gate connection will be discussed for the charge partition input CCD delay lines.

1. Input Control Gate

The 'control gate #1' and 'control gate #3' connections of the input structure are the only items connected to the *input control gate bond pad.* The input control gates are located between the input diffusion region and the first gate electrode of the CCD register. The input control gates are held at a constant high voltage, +5 volts. With a +5 voltage on these control gates, carriers can fill in the potential well region under the gates. This connection for these two control gates could be made the same as VDD.

2. P Diffusion Stop/ No P Diffusion Stop

On each chip there are two CCD delay lines which have charge partition input structures. One of these delay lines has a P diffusion stop for lateral charge confinement and one does not. The two delay lines share all the same bond pads except for the 'signal

in' and 'signal out'. Once satisfactory CCD operation is achieved, these two different CCD delay lines should be compared in testing.

VI. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

A chip with four variants of a bulk-channel charge-coupled device (BCCD) analog delay line has been designed using the design tools currently available at NPS. The design for the digital portions of the chip such as the on-chip clock, clock output driver, and output amplifier were simulated to verify the functional operation and to confirm proper layout. NPS simulation tools simulate transistor-based circuits and do not allow for the simulation of CCD structures. Given this restriction, conservative CCD parameters were used in the design to ensure CCD delay will operate correctly.

B. RECOMMENDATIONS

1) Test the chip, when it returns from fabrication, to determine which of the four CCD delay line variants provides the best operating characteristics.

2) Design an optically stimulated CCD delay, which would lead the way to designing an optical array.

3) Investigate to determine whether the new CAD tool Cadence provides any new capabilities with regards to designing CCDs.

APPENDIX A: ON-CHIP CLOCK CIRCUIT DESIGN

A. CLOCK CIRCUIT STATE DIAGRAM

Figure 38 show the state diagram for the four-phase clock circuit. The clock circuit is a continuous loop of four states. It advances to the next state when pulsed by the master clock signal, which comes from off-chip.

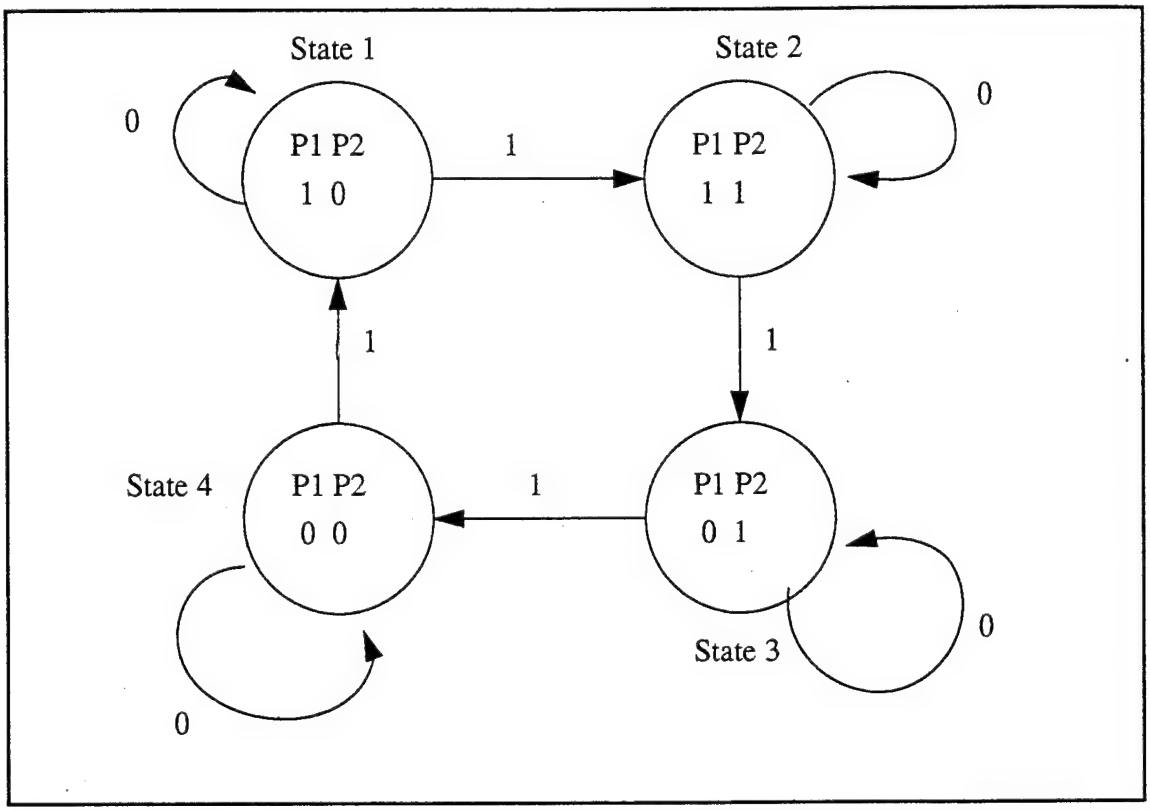

Figure 38. State Diagram for CCD Clock Circuit.

B. CLOCK CIRCUIT STATE TABLE

Below is the state table describing the state diagram in Figure 38. From the state table, equations for DØ1 and DØ2 are determined. Since Ø3 is the complement of Ø1 and Ø4 is the complement of Ø2, only two equations, vice four, are needed.

Present State		Input	Next State		Output	
P1	P2	X	P1	P2	P1	P2
0	0	0	0	0	0	0
0	0	1	1	0	1	0
0	1	0	0	1	0	1
0	1	1	0	0	0	0
1	0	0	1	0	1	0
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	0	1	0	1

D Ø1 (P1, P2, X) = $\sum$ (1, 4, 5, 6)
D Ø2 (P1, P2, X) = $\sum$ (2, 5, 6, 7)

C. CLOCK CIRCUIT KARNOUGH MAPS

Below are shown the karnough maps for the equations describing DØ1 and DØ2.

Ø1 \ Ø2 X	00	01	11	01
0	0	1	0	0
1	1	1	0	1

D Ø1 = Ø2 X + Ø1 X

Ø1 \ Ø2 X	00	01	11	01
0	0	0	0	1
1	0	1	1	1

D Ø2 = Ø1 X + Ø2 X

D. DERIVED CLOCK CIRCUIT

The schematic in Figure 39 is the clock circuit derived from the above equations. This circuit was drawn and logically simulated using the B2 Logic program. Figure 40 shows the timing trace diagram for the clocking circuit.

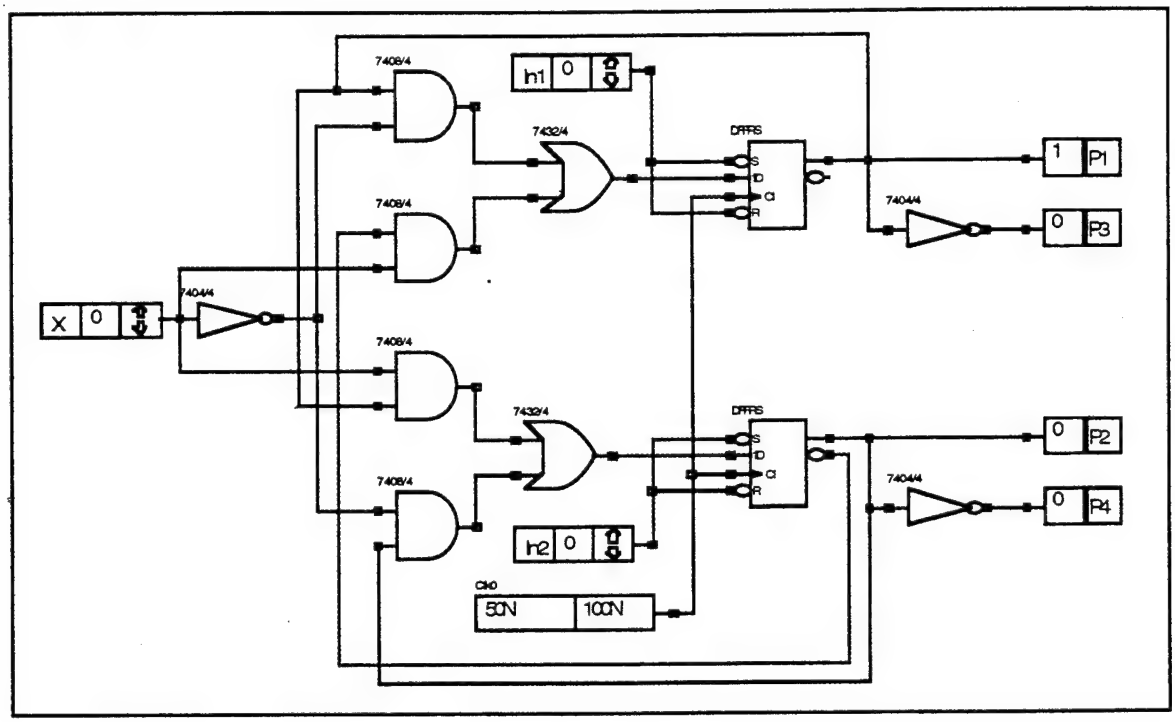

Figure 39. Schematic of Derived CCD Clock Circuit.

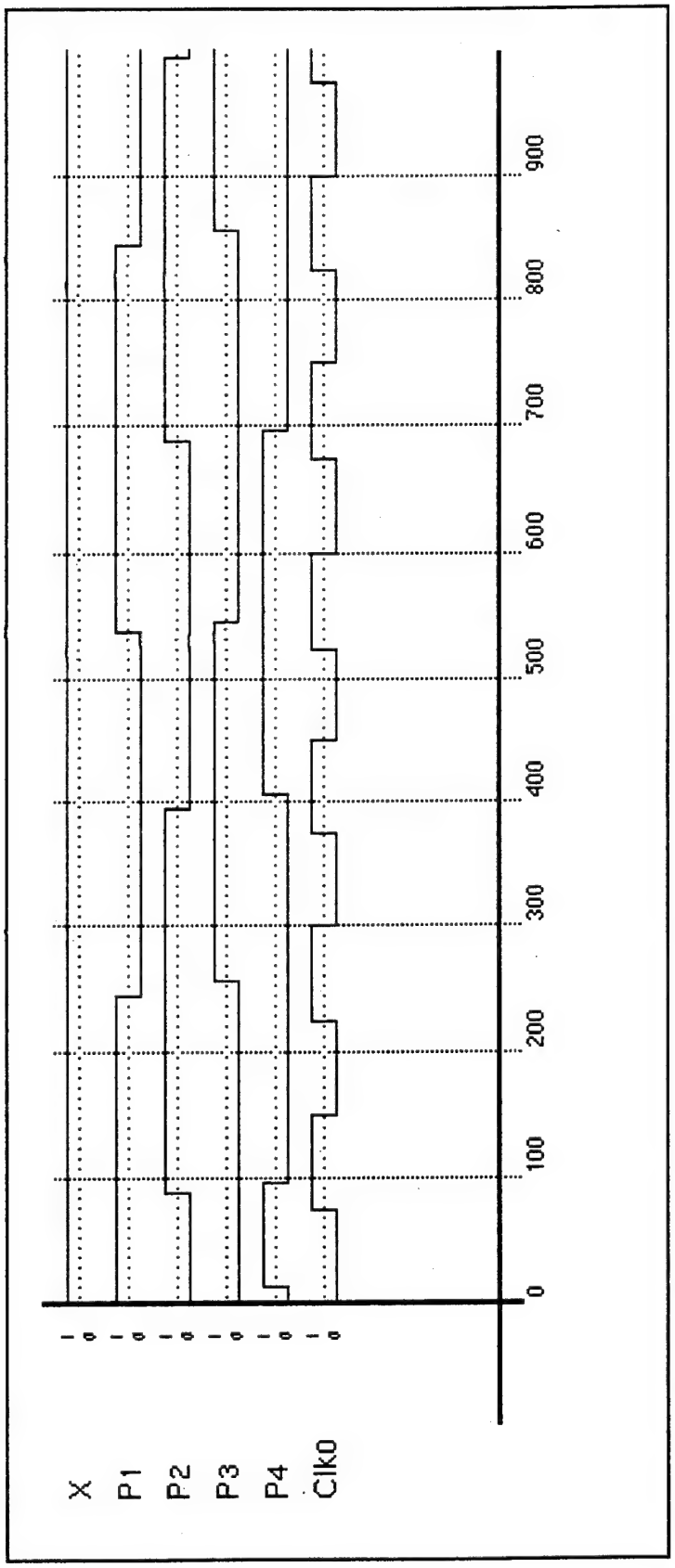

Figure 40. Timing Traces of Clock Circuit from B2 Logic Program.

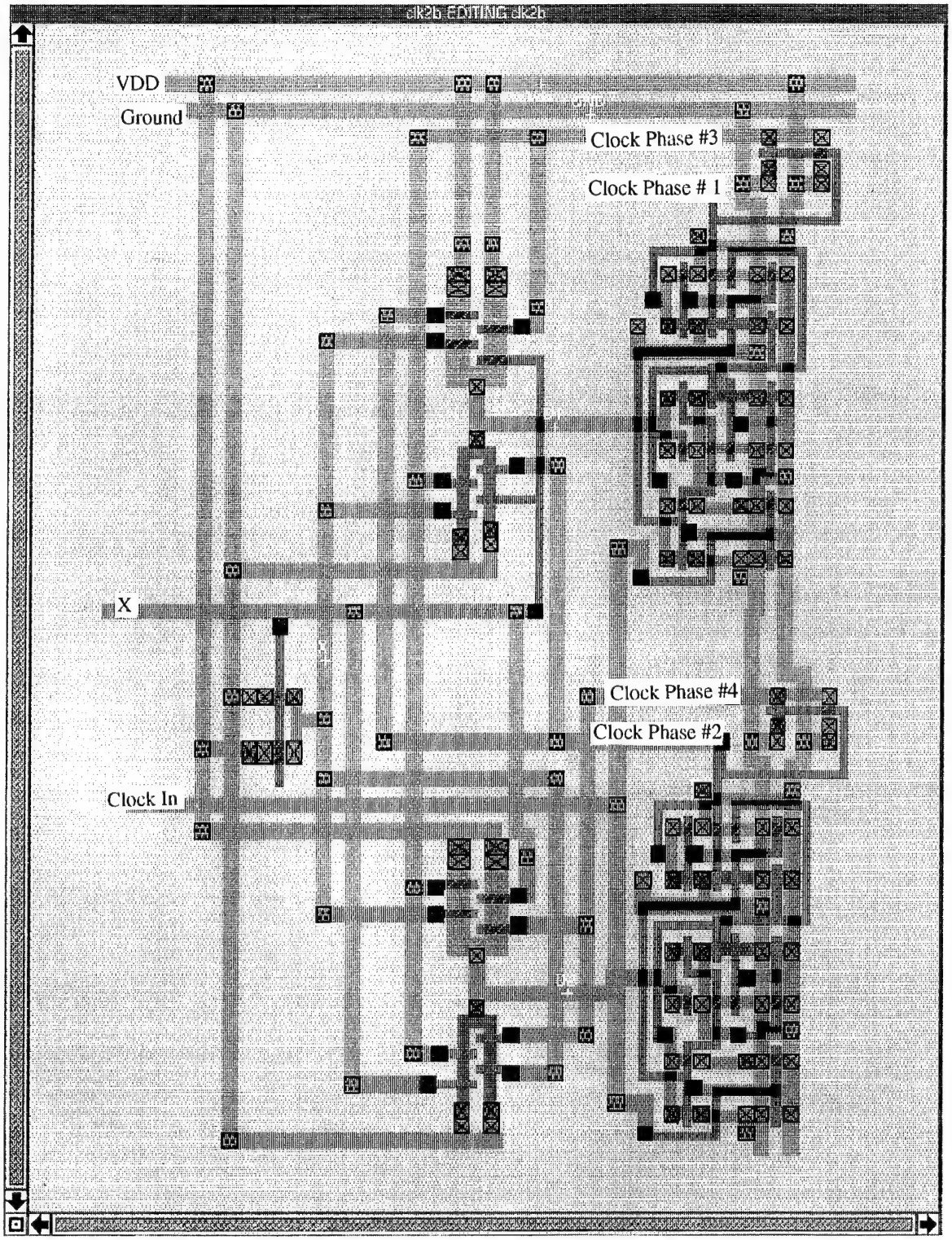

Figure 41. On-Chip Clock Circuit.

F. FINITE STATE MACHINE SIMULATION

Below is the ESIM simulation of the extracted Magic clock cell layout. The output matches the desired state diagram in Figure 30.

```
sun10:/home5/gedra/Thesis_Clock/CLK
% esim clk1.sim
ESIM  (V3.5 03/27/91)
62 transistors, 37 nodes (0 pulled up)
sim> w CLK P1 P2 P1Not P2Not
sim> V X 11111111111111111111111111111111111111
sim> V D1 1XXXXXXXXXXXXXXXXXXXXXXXXXXX
sim> V D2 1XXXXXXXXXXXXXXXXXXXXXXXXXXX
sim> CLK 10101010101010101010101010101010101010101010
sim> I
initialization took 46 steps
sim> I
initialization took 0 steps
sim> G
>11000011110000111100001111000011110000011 : P1
>11110000111100001111000011110000111100000 : P2
>00111100001111000011110000111100001111100 : P3
>00001111000011110000111100001111000011111 : P4
sim>quit
```

APPENDIX B: CLOCK SIGNAL DRIVER DESIGN

A. STAGE RATIO

As described in Chapter III, the clock driver circuit has to drive the input structure, all the gate electrodes and the output structure of the CCD analog delay line. In order to drive this large capacitive load, the output clock signals are passed through a chain of inverters where each successive inverter is made larger than the previous one. The last inverter through which the signal passes is sufficiently large enough to drive the capacitive load in the time required. The ratio by which each stage is increased in size is called the stage ratio, denoted by *a*.

The stage ratio circuit in Figure 42 consist of four cascaded inverters with a stage ratio *a*, which are driving a capacitance load C_L. The first inverter is a minimum-sized inverter driving the second inverter, which is *a* times the size of the minimum size inverter. Likewise, the second inverter drives the third inverter, which is a^2 times the size of the minimum inverter. If *n* is the number of inverter stages and C_x is the capacitance of a minimum size inverter, then a sufficient number of inverter stages are placed in the stage ratio circuit so that $a^n C_x = C_L$.

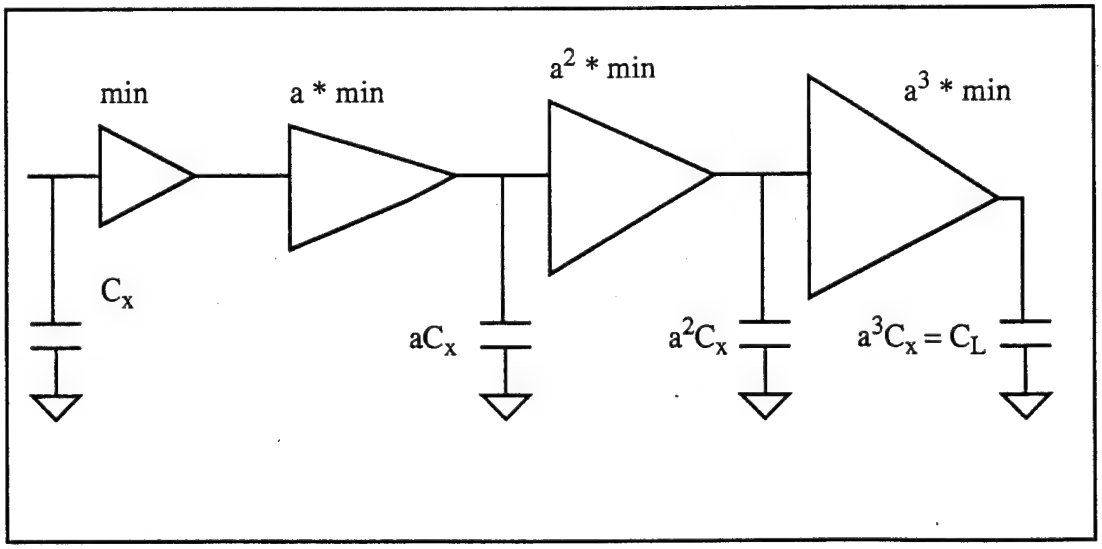

Figure 42. Stage Ratio Circuit.

The optimum stage ratio is determined from equation (11)

$$a_{opt} = e^{(k + a_{opt}) / (a_{opt})} \qquad (11)$$

where k is the ratio of the intrinsic output load capacitance to the input gate capacitance of a minimum sized inverter, as shown in equation (12).

$$k = \frac{C_{drain}}{C_{gate}} \qquad (12)$$

B. CAPACITANCE ESTIMATION

The first piece of information needed is an estimation of the capacitance associated with a minimum sized inverter, C_x. Figure 43 shows the dimensions associated with a minimum inverter for the Orbit CMOS process. The units of length are micrometers, μm. The capacitances used in the calculations come from the Orbit nwell specifications and from Table 4.6 of reference 19, where Orbit specifications were not available.

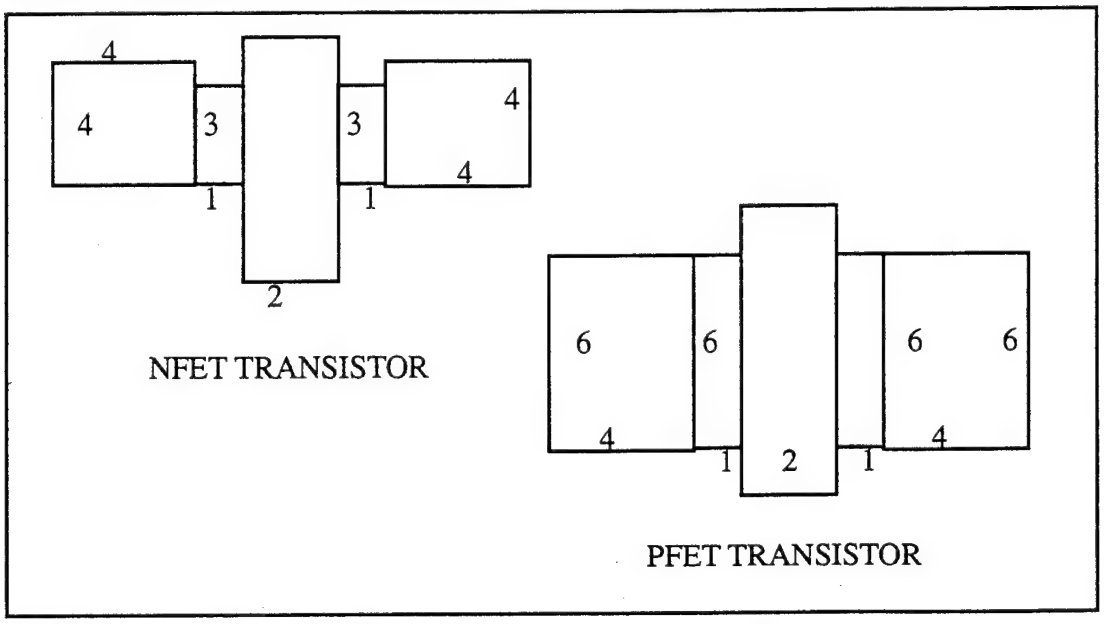

Figure 43. Dimension of Transistors in a Minimum Size Inverter.

The capacitance of the gate is simply the parallel plate capacitance while the capacitance of the drain is the parallel plate plus the periphery capacitances. Therefore the estimated capacitances of the NFET portion of the inverter are as follows:

C_{gate}= (2*3) (900E-18) = 5.40E-15 F

C_{drain} = [2 * ((4 * 4) + (1 * 3)) * 150E-18] + [2 * (4 + 4 +1 + 3 +1 + 4) * 200E-18]

= 1.29E-14 F

The estimated capacitances of the PFET portion of the inverter are:

C_{gate} = (2 * 6) (900E-14) = 1.08E-14 F

C_{drain} = [2 * ((4 * 6) + (1 * 6)) * 250E-18] + [2 * (6 + 4 + 1 + 6 +1 + 4) * 200E-18]

= 2.38E-14 F

Using equation (12), $k = \frac{C_{drain}}{C_{gate}} = \frac{\left(1.29\times10^{-14} + 2.38\times10^{-14}\right)}{5.40\times10^{-15} + 1.08\times10^{-14}} = 2.2654$. Now, a_{opt} can be determined by using equation (11), $a_{opt} = e^{\frac{k + a_{opt}}{a_{opt}}} = e^{\frac{2.2654 + a_{opt}}{a_{opt}}} = 4.498$, which means each successive stage is 4.498 times larger than the previous. From the above capacitance estimations, the total capacitance of the minimum inverter, C_x, can be estimated:

$C_x = C_{NFETGate} + C_{NFETDrain} + C_{PFETGate} + C_{PFETDrain}$

= 5.40E-15 + 1.29E-14 + 1.08E-14 + 2.38E-14

= 5.29E-14 F

C. NUMBER OF STAGES

With the information obtained in the last subsection, we can now determine the number of inverter stages necessary to drive the capacitive load of the CCD delay line. Table 1 summarizes the transistor sizes and capacitance loads for each stage.

Stage	Capacitance Symbol	Capacitance Estimation (Farads)	NFET Width (μm)	PFET Width (μm)
1	C_x	5.29E-14	3	6
2	aC_x	2.38E-13	14	27
3	a^2C_x	1.07E-12	61	122
4	a^3C_x	4.81E-12	273	546
5	a^4C_x	2.17E-11	1228	2456

Table 1: Stage Ratio Capacitance & Transistor Size Summary

As can be observed from the table, the NFET and PFET sizes for a five stage inverter chain are prohibitively large for this chip design; they would consume a great portion of the available die area. The transistor sizes for the four stage inverter chain are more reasonable with our given size restrictions.

To check whether the four stage inverter chain could drive the capacitive load of the CCD register, the capacitive load, C_L, was estimated from the CCD analog delay line design. C_L was estimated as follows:

- C of metal 2 run = [(4 μm * 1718 μm) - ((4 μm * 4 μm) * 64)) * 10E-18 F/μm]
  = 5.848E-14 F
- C of metal 2 to metal 1 = (4 μm * 4μm) * 64 * 25E-18 F/μm^2 = 2.560E-14 F
- C of metal 1 to substrate = 64 * 18 μm^2 * 15E-18 F/μm^2 = 1.728E-14 F
- C metal 1 to diffusion = 64 * 9 μm^2 * 30E-18 F/μm^2 = 1.728E-14 F
- C poly to substrate = 64 * 69 μm^2 * 25E-18 F/μm^2 = 1.104E-13 F
- C poly to BCC diffusion = 64 * 80 μm^2 * 9.0E-16 F/μm^2 = 4.608E-12 F

C_L = 4.837E-12 F

The estimated value of 4.837E-12 F for C_L compares well with the 4.814E-12 F for the estimated a^3C_x that a four stage inverter chain is capable of driving.

D. MAGIC LAYOUT OF THE CLOCK SIGNAL DRIVER

From Table 1, one can see that both the NFET and PFET widths of the final stage of the inverter chain become very large. The transistor gate width for the NFET is 273 μm and 546 μm for the PFET to drive the load capacitance. All transistors with gate widths in excess of 75 microns are constructed as multi-fingered transistors using parallel gates with widths less than 75 microns, as shown in the Clock Output Driver layout in Figure 44. The minimum size width for the power and ground conductors is chosen such that the current density of the particular conductor will not exceed the current limit. Exceeding the current limit can cause electromigration, which is the migration of metal ions in the conductor away from the high current density. Electromigration can eventually cause an opening in the conductor, rendering the circuit useless. Spice simulation results from the original design files are used for determining the minimum widths. A current limit of 0.6 milliamperes per micron of width is used for metal one and 1.15 milliamperes per micron width is used for metal two.

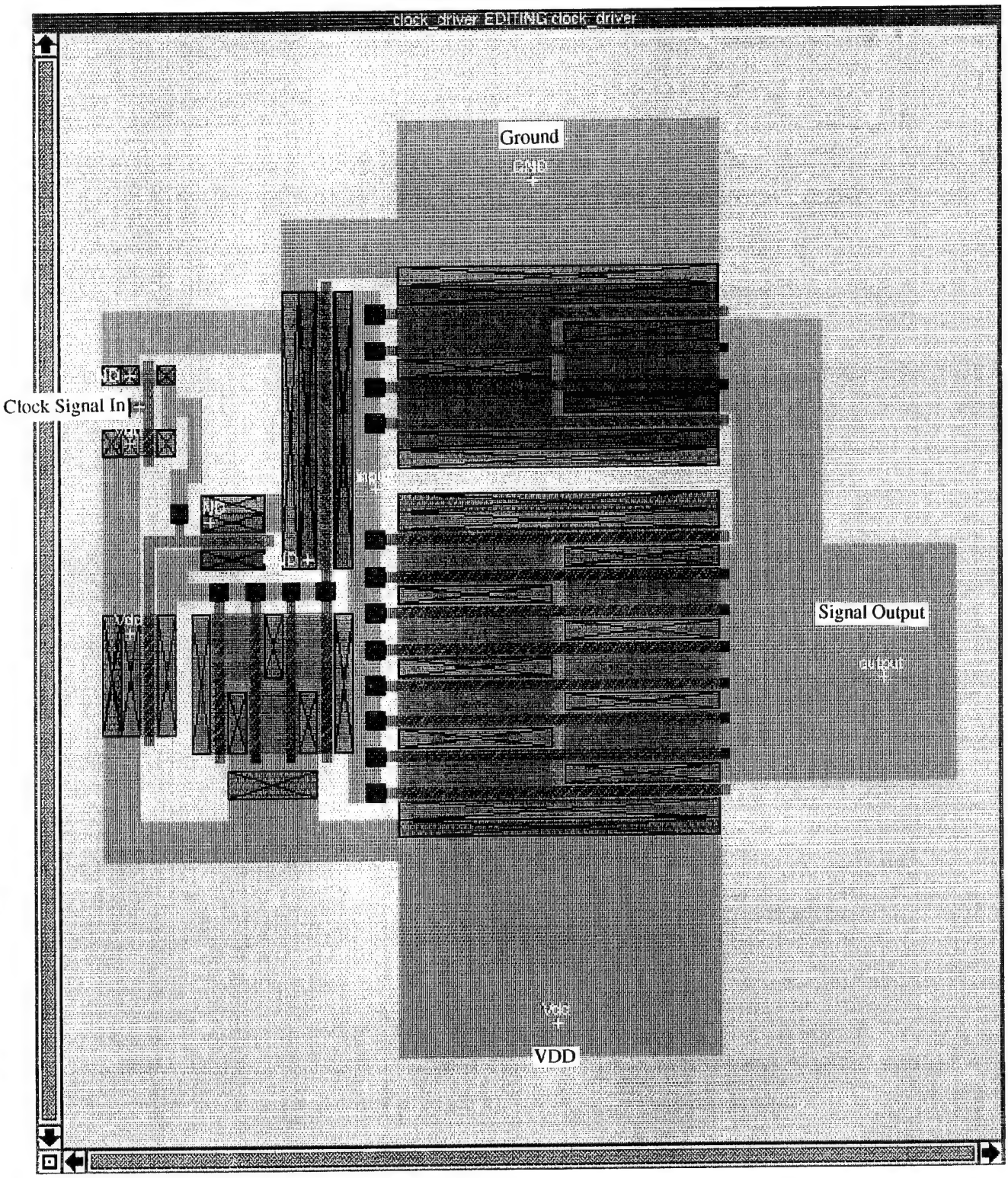

Figure 44. Clock Signal Driver Circuit.

E. EXTRACTED FILE FROM CLOCK SIGNAL DRIVER LAYOUT

```
timestamp 794534666
version 5.0
tech scmos
scale 1000 1000 100
resistclasses 38400 130400 25300 25300 49 33 2776000 3000000
node "Vdd!" 16512 836 -21 2 nnc 948 522 2649 1070 0 0 0 0 4187 896 0 0 0 0 0 0
node "output" 7989 857 128 -68 pdiff 852 308 1704 616 0 0 0 0 8219 1140 0 0 0 0 0 0
node "OUT3" 2119 253 52 -30 pdiff 305 132 372 148 0 0 0 0 1609 490 0 0 0 0 0 0
node "OUT2" 812 81 26 -19 pdiff 70 38 135 64 0 0 0 0 52 34 0 0 0 0 0 0
node "OUT1" 221 29 -10 2 pdiff 19 18 30 22 0 0 0 0 62 42 0 0 0 0 0 0
node "IN1" 378 6 -19 11 pc 0 0 0 0 68 68 0 0 0 0 0 0 0 0 0 0
node "GND!" 10847 433 -21 18 ppc 1530 646 884 482 0 0 0 0 2941 622 0 0 0 0 0 0
node "IN2" 784 7 17 11 pc 0 0 0 0 132 132 0 0 40 28 0 0 0 0 0 0
node "IN3" 3113 19 46 11 pc 0 0 0 0 508 504 0 0 120 92 0 0 0 0 0 0
node "IN4" 12701 52 125 6 pc 0 0 0 0 2016 2016 0 0 608 168 0 0 0 0 0 0
cap "GND!" "output" 29
cap "IN4" "output" 1
cap "OUT3" "Vdd!" 12
cap "output" "Vdd!" 67
fet pfet 182 -68 183 -67 142 146 "Vdd!" "IN4" 4 0 "output" 71 0 "Vdd!" 71 0
fet pfet 174 -68 175 -67 142 146 "Vdd!" "IN4" 4 0 "Vdd!" 71 0 "output" 71 0
fet pfet 166 -68 167 -67 142 146 "Vdd!" "IN4" 4 0 "output" 71 0 "Vdd!" 71 0
fet pfet 158 -68 159 -67 142 146 "Vdd!" "IN4" 4 0 "Vdd!" 71 0 "output" 71 0
fet pfet 150 -68 151 -67 142 146 "Vdd!" "IN4" 4 0 "output" 71 0 "Vdd!" 71 0
fet pfet 142 -68 143 -67 142 146 "Vdd!" "IN4" 4 0 "Vdd!" 71 0 "output" 71 0
fet pfet 134 -68 135 -67 142 146 "Vdd!" "IN4" 4 0 "output" 71 0 "Vdd!" 71 0
fet pfet 126 -68 127 -67 142 146 "Vdd!" "IN4" 4 0 "Vdd!" 71 0 "output" 71 0
fet pfet 74 -30 75 -29 62 66 "Vdd!" "IN3" 4 0 "OUT3" 31 0 "Vdd!" 31 0
fet pfet 66 -30 67 -29 62 66 "Vdd!" "IN3" 4 0 "Vdd!" 31 0 "OUT3" 31 0
fet pfet 58 -30 59 -29 62 66 "Vdd!" "IN3" 4 0 "OUT3" 31 0 "Vdd!" 31 0
fet pfet 50 -30 51 -29 62 66 "Vdd!" "IN3" 4 0 "Vdd!" 31 0 "OUT3" 31 0
fet pfet 24 -19 25 -18 54 58 "Vdd!" "IN2" 4 0 "Vdd!" 27 0 "OUT2" 27 0
fet pfet -12 2 -11 3 12 16 "Vdd!" "IN1" 4 0 "Vdd!" 6 0 "OUT1" 6 0
fet nfet 156 25 157 26 142 146 "GND!" "IN4" 4 0 "output" 71 0 "GND!" 71 0
fet nfet 148 25 149 26 142 146 "GND!" "IN4" 4 0 "GND!" 71 0 "output" 71 0
fet nfet 140 25 141 26 142 146 "GND!" "IN4" 4 0 "output" 71 0 "GND!" 71 0
fet nfet 132 25 133 26 142 146 "GND!" "IN4" 4 0 "GND!" 71 0 "output" 71 0
fet nfet 50 18 51 19 122 126 "GND!" "IN3" 4 0 "GND!" 61 0 "OUT3" 61 0
fet nfet 24 18 25 19 28 32 "GND!" "IN2" 4 0 "GND!" 14 0 "OUT2" 14 0
fet nfet -12 18 -11 19 6 10 "GND!" "IN1" 4 0 "GND!" 3 0 "OUT1" 3 0
```

F. CLOCK SIGNAL DRIVER SPICE FILE READY FOR SIMULATION

```
 SPICE File for Driver

.MODEL nnf NMOS LEVEL=2 PHI=0.600000 TOX=4.2100E-08 XJ=0.200000U TPG=1
+ VTO=0.8673 DELTA=4.9450E+00 LD=3.5223E-07 KP=4.6728E-05
+ UO=569.7 UEXP=1.7090E-01 UCRIT=5.9350E+04 RSH=1.9090E+01
+ GAMMA=0.4655 NSUB=4.3910E+15 NFS=1.980E+11 VMAX=5.7510E+04
+ LAMBDA=3.9720E-02 CGDO=4.3332E-10 CGSO=4.3332E-10
+ CGBO=3.5977E-10 CJ=1.0096E-04 MJ=0.8119 CJSW=4.6983E-10
+ MJSW=0.323107 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -9.0180E-08

.MODEL npf PMOS LEVEL=2 PHI=0.600000 TOX=4.2100E-08 XJ=0.200000U TPG=-1
+ VTO=-0.9506 DELTA=4.5950E+00 LD=3.7200E-07 KP=1.6454E-05
+ UO=200.6 UEXP=2.6690E-01 UCRIT=7.9260E+04 RSH=4.9920E+01
+ GAMMA=0.6561 NSUB=8.7250E+15 NFS=3.27E+11 VMAX=9.9990E+05
+ LAMBDA=4.5950E-02 CGDO=4.5769E-10 CGSO=4.5769E-10
+ CGBO=3.8123E-10 CJ=3.1469E-04 MJ=0.5687 CJSW=3.1456E-10
+ MJSW=0.275802 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -2.2400E-07

** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 2 = Error

Vdd 1 0 5.0
Vin 101 0

VM1 100 103 0.0
VM2 102 105 0.0
VM3 104 107 0.0

** SPICE file created for circuit drtest
** Technology: scmos
**

** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 2 = Error
M0 100 101 0 0 nnf L=2.0U W=3.0U
M1 102 103 0 0 nnf L=2.0U W=14.0U
M2 104 105 0 0 nnf L=2.0U W=61.0U
M3 106 107 0 0 nnf L=2.0U W=71.0U
M4 0 107 106 0 nnf L=2.0U W=71.0U
M5 106 107 0 0 nnf L=2.0U W=71.0U
M6 0 107 106 0 nnf L=2.0U W=71.0U
M7 100 101 1 1 npf L=2.0U W=6.0U
```

```
M8 102 103 1 1 npf L=2.0U W=27.0U
M9 104 105 1 1 npf L=2.0U W=31.0U
M10 1 105 104 1 npf L=2.0U W=31.0U
M11 104 105 1 1 npf L=2.0U W=31.0U
M12 1 105 104 1 npf L=2.0U W=31.0U
M13 106 107 1 1 npf L=2.0U W=71.0U
M14 1 107 106 1 npf L=2.0U W=71.0U
M15 106 107 1 1 npf L=2.0U W=71.0U
M16 1 107 106 1 npf L=2.0U W=71.0U
M17 106 107 1 1 npf L=2.0U W=71.0U
M18 1 107 106 1 npf L=2.0U W=71.0U
M19 106 107 1 1 npf L=2.0U W=71.0U
M20 1 107 106 1 npf L=2.0U W=71.0U

RLOAD 104 0 100000

C0 104 1 12F
C1 1 0 836F
** NODE: 1 = Vdd!
C2 106 0 886F
** NODE: 106 = output
C3 104 0 253F
** NODE: 104 = OUT3
C4 102 0 81F
** NODE: 102 = OUT2
C5 100 0 29F
** NODE: 100 = OUT1
** NODE: 101 = IN1
** NODE: 0 = GND!
** NODE: 103 = IN2
C6 105 0 19F
** NODE: 105 = IN3
C7 107 0 52F
** NODE: 107 = IN4

.options dcon=1 post

.DC Vin 0 5 0.5

.meas avg_power avg power
.meas max_power max power

*.PRINT DC I(VM1) I(VM2) I(VM3) I(RLOAD)

.END
```

G. HSPICE SIMULATION RESULTS

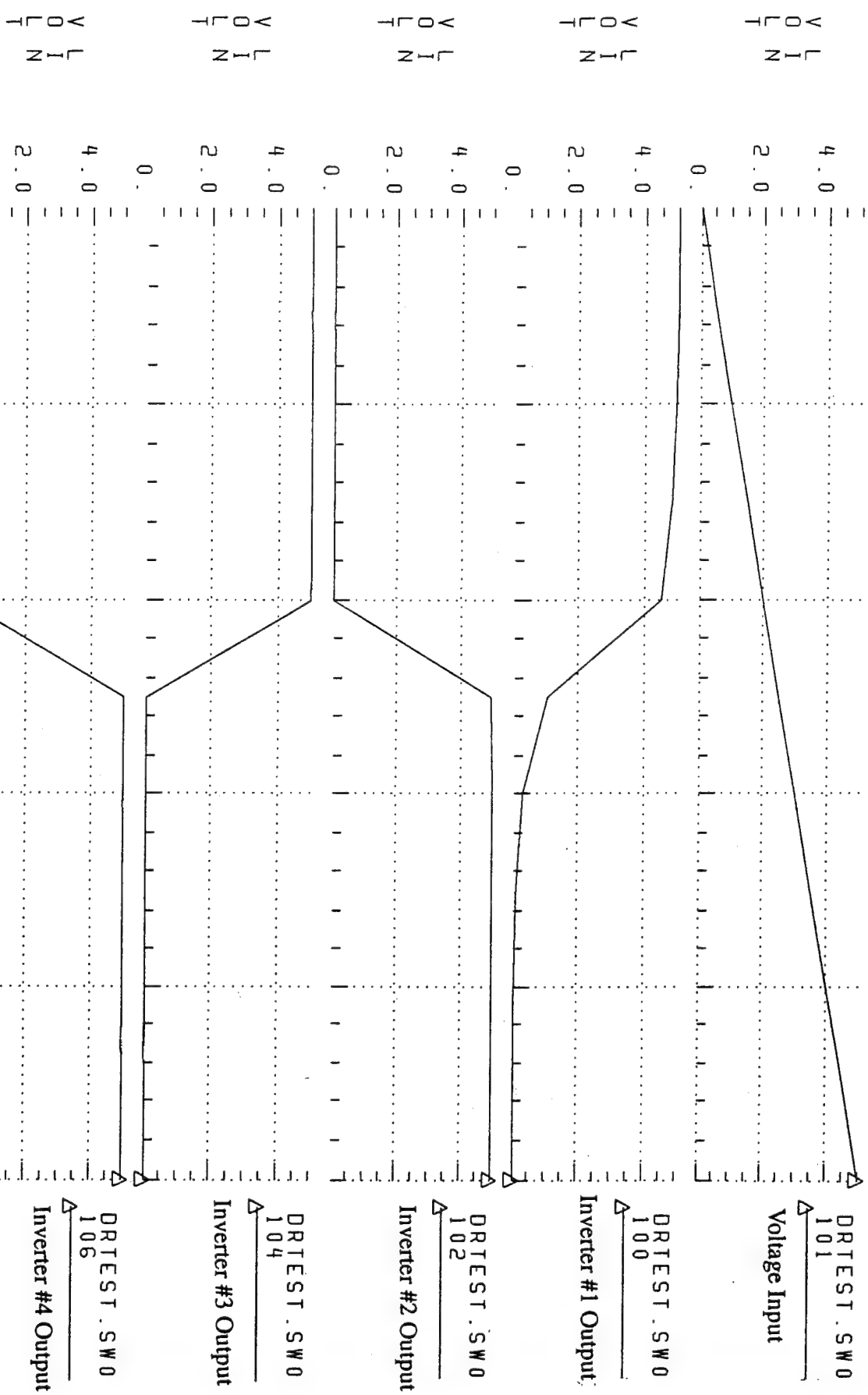

Figure 45. HSPICE Simulation Results for Clock Signal Driver Circuit.

APPENDIX C: OUTPUT SENSE AMPLIFIER

As was discussed in Chapter III, the output signal from the CCD must be sufficiently amplified after it has been detected to be useful. Therefore, an on-chip amplifier with low noise and high gain was desired. A differential amplifier was chosen as the type of amplifier to design with.

A. DIFFERENTIAL AMPLIFIER

An active-loaded CMOS differential amplifier is shown if Figure 46. It consists of an NFET differential pair M3 and M4 loaded by the current mirror formed by PFET transistors M1 and M2. The current mirror consisting of NFET transistors M5 and M6 provide a constant current source to the sources of M3 and M4. An input signal Vin from the CCD register is applied to the base of M3, while a dc bias voltage Vref is applied to the base of M4. The dc bias voltage can be adjusted from an off-chip source.

B. MAGIC LAYOUT OF THE DIFFERENTIAL AMPLIFIER

The Magic layout of the active-loaded differential amplifier is shown in Figure 47. The widths of the differential pair transistors were determined to be 50 μm. To minimize the die area required for the differential amplifiers, multi-finger transistors with gate widths of 13 μm were used in the design.

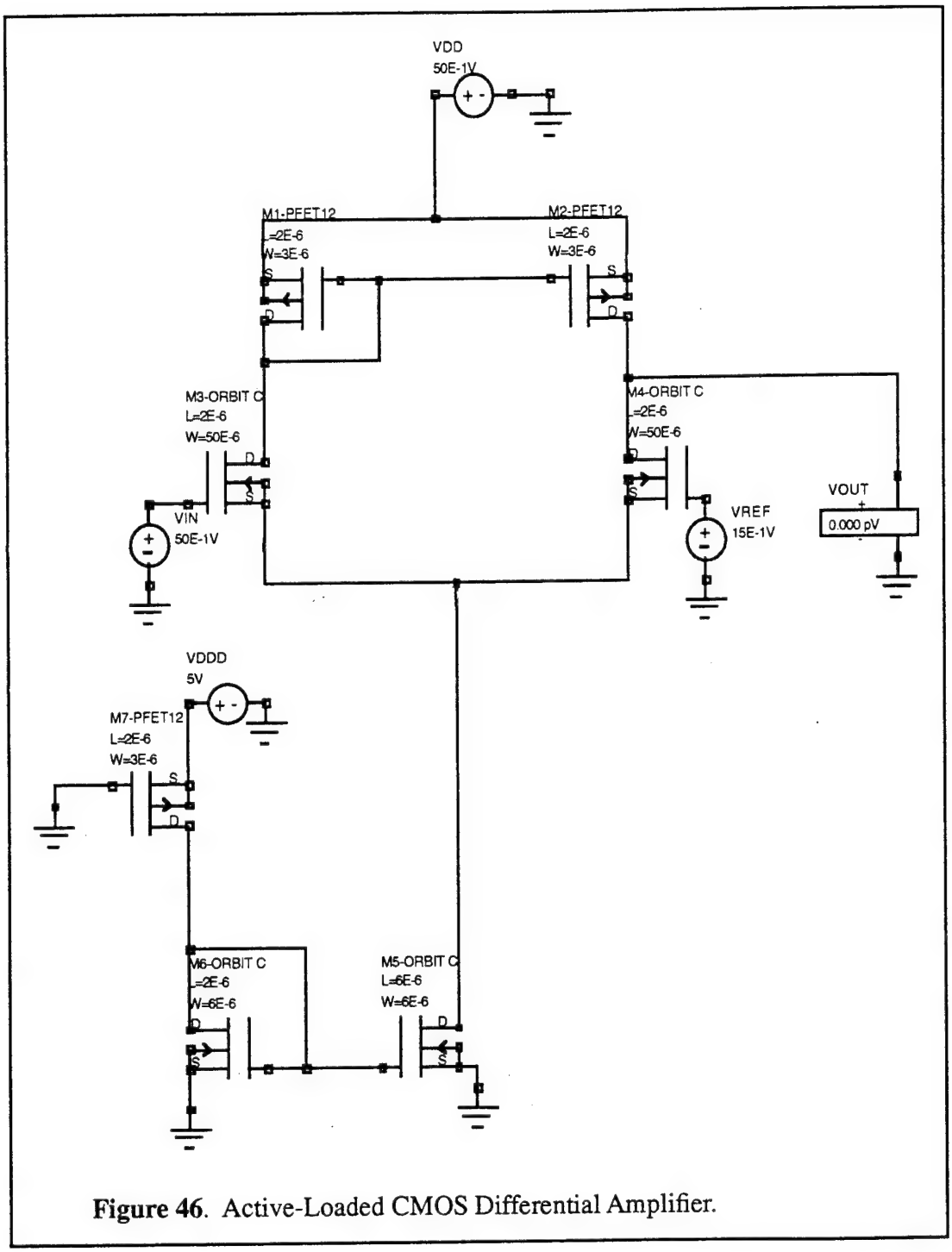

Figure 46. Active-Loaded CMOS Differential Amplifier.

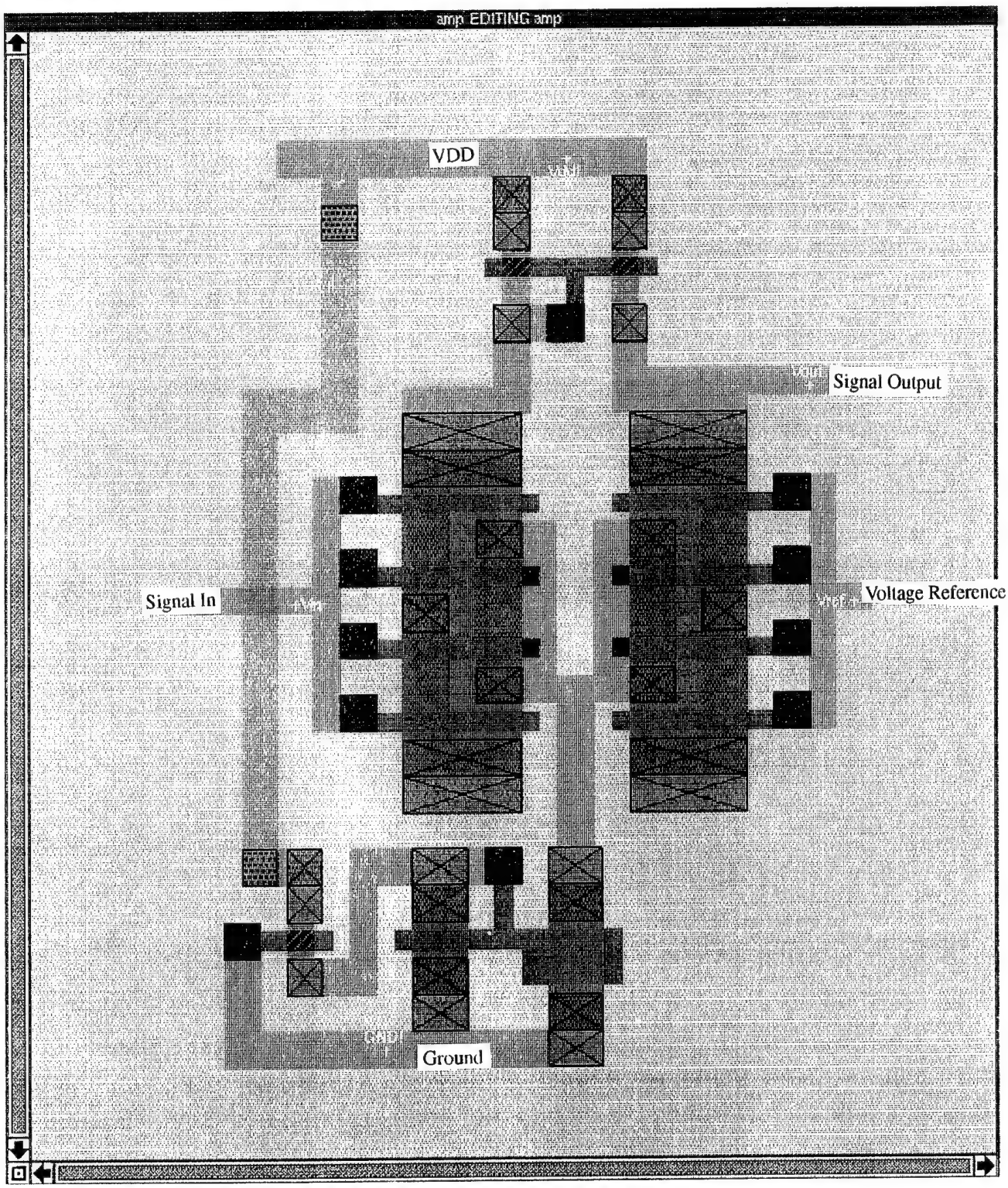

Figure 47. Magic Layout of the Active-Loaded Differential Amplifier.

C. EXTRACTED FILE FROM DIFFERENTIAL AMPLIFIER LAYOUT

```
timestamp 795202290
version 5.0
tech scmos
scale 1000 1000 100
resistclasses 38400 130400 25300 25300 49 33 2776000 3000000
node "GND!" 1179 32 -55 -40 pc 60 44 48 40 32 32 0 0 176 96 0 0 0 0 0 0
node "8_97_89#" 1179 33 -48 -44 pdc 30 22 43 38 120 84 0 0 84 64 0 0 0 0 0 0
node "8_71_27#" 967 114 -35 -13 ndiff 342 174 24 20 0 0 0 0 356 150 0 0 0 0 0 0
node "Vref" 1265 15 -12 -15 p 0 0 0 0 208 208 0 0 96 70 0 0 0 0 0 0
node "Vin" 1265 16 -42 -15 pc 0 0 0 0 208 208 0 0 141 100 0 0 0 0 0 0
node "Vout" 2256 82 -12 28 pdc 208 110 129 90 0 0 0 0 240 136 0 0 0 0 0 0
node "8_71_49#" 2583 87 -35 -24 ppc 208 110 129 90 60 60 0 0 190 124 0 0 0 0 0 0
node "Vdd!" 1776 39 -48 -37 pdiff 48 48 57 54 0 0 0 0 212 122 313 160 0 0 0 0
cap "Vout" "8_71_27#" 4
cap "Vdd!" "Vin" 1
cap "8_71_49#" "8_71_27#" 4
fet nfet -19 -43 -18 -42 36 24 "GND!" "8_97_89#" 12 0 "GND!" 6 0 "8_71_27#" 6 0
fet nfet -34 -39 -33 -38 12 16 "GND!" "8_97_89#" 4 0 "GND!" 6 0 "8_97_89#" 6 0
fet pfet -48 -39 -47 -38 6 10 "Vdd!" "GND!" 4 0 "8_97_89#" 3 0 "Vdd!" 3 0
fet nfet -10 -15 -9 -14 26 30 "GND!" "Vref" 4 0 "Vout" 13 0 "8_71_27#" 13 0
fet nfet -35 -15 -34 -14 26 30 "GND!" "Vin" 4 0 "8_71_49#" 13 0 "8_71_27#" 13 0
fet nfet -10 -7 -9 -6 26 30 "GND!" "Vref" 4 0 "8_71_27#" 13 0 "Vout" 13 0
fet nfet -35 -7 -34 -6 26 30 "GND!" "Vin" 4 0 "8_71_27#" 13 0 "8_71_49#" 13 0
fet nfet -10 1 -9 2 26 30 "GND!" "Vref" 4 0 "Vout" 13 0 "8_71_27#" 13 0
fet nfet -35 1 -34 2 26 30 "GND!" "Vin" 4 0 "8_71_49#" 13 0 "8_71_27#" 13 0
fet nfet -10 9 -9 10 26 30 "GND!" "Vref" 4 0 "8_71_27#" 13 0 "Vout" 13 0
fet nfet -35 9 -34 10 26 30 "GND!" "Vin" 4 0 "8_71_27#" 13 0 "8_71_49#" 13 0
fet pfet -12 35 -11 36 6 10 "Vdd!" "8_71_49#" 4 0 "Vout" 3 0 "Vdd!" 3 0
fet pfet -24 35 -23 36 6 10 "Vdd!" "8_71_49#" 4 0 "8_71_49#" 3 0 "Vdd!" 3 0
```

D. DIFFERENTIAL AMPLIFIER SPICE FILE READY FOR SIMULATION

```
SPICE file created for circuit amp
** Technology: scmos
**
.MODEL nnf NMOS LEVEL=2 PHI=0.600000 TOX=4.2100E-08 XJ=0.200000U TPG=1
+ VTO=0.8673 DELTA=4.9450E+00 LD=3.5223E-07 KP=4.6728E-05
+ UO=569.7 UEXP=1.7090E-01 UCRIT=5.9350E+04 RSH=0.0000
+ GAMMA=0.4655 NSUB=4.3910E+15 NFS=1.980E+11 VMAX=5.7510E+04
+ LAMBDA=3.9720E-02 CGDO=4.3332E-10 CGSO=4.3332E-10
+ CGBO=3.5977E-10 CJ=1.0096E-04 MJ=0.8119 CJSW=4.6983E-10
+ MJSW=0.323107 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -9.0180E-08

.MODEL npf PMOS LEVEL=2 PHI=0.600000 TOX=4.2100E-08 XJ=0.200000U TPG=-1
+ VTO=-0.9506 DELTA=4.5950E+00 LD=3.7200E-07 KP=1.6454E-05
+ UO=200.6 UEXP=2.6690E-01 UCRIT=7.9260E+04 RSH=0.0000
+ GAMMA=0.0000 NSUB=8.7250E+15 NFS=3.27E+11 VMAX=9.9990E+05
+ LAMBDA=4.5950E-02 CGDO=4.5769E-10 CGSO=4.5769E-10
+ CGBO=3.8123E-10 CJ=3.1469E-04 MJ=0.5687 CJSW=3.1456E-10
+ MJSW=0.275802 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -2.2400E-07

** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 2 = Error

Vdd 1 0 5.0
Vin 102 0
Vref 104 0 1.75


M0 1 100 100 1 npf L=2.0U W=3.0U
M1 1 100 101 1 npf L=2.0U W=3.0U
M2 100 102 103 0 nnf L=2.0U W=13.0U
M3 101 104 103 0 nnf L=2.0U W=13.0U
M4 103 102 100 0 nnf L=2.0U W=13.0U
M5 103 104 101 0 nnf L=2.0U W=13.0U
M6 100 102 103 0 nnf L=2.0U W=13.0U
M7 101 104 103 0 nnf L=2.0U W=13.0U
M8 103 102 100 0 nnf L=2.0U W=13.0U
M9 103 104 101 0 nnf L=2.0U W=13.0U
M10 1 0 105 1 npf L=2.0U W=3.0U
M11 105 105 0 0 nnf L=2.0U W=6.0U
M12 103 105 0 0 nnf L=6.0U W=6.0U

** NODE: 0 = GND!
C0 105 0 33F
```

```
** NODE: 105 = 8_97_89#
C1 103 0 114F
** NODE: 103 = 8_71_27#
C2 104 0 15F
** NODE: 104 = Vref
C3 102 0 16F
** NODE: 102 = Vin
C4 101 0 82F
** NODE: 101 = Vout
C5 100 0 87F
** NODE: 100 = 8_71_49#
C6 1 0 39F
** NODE: 1 = Vdd!

.options post

.DC Vin 0 5.0 0.05

.meas avg_power avg power
.meas max_power max power

.END
```

E. HSPICE SIMULATION RESULTS

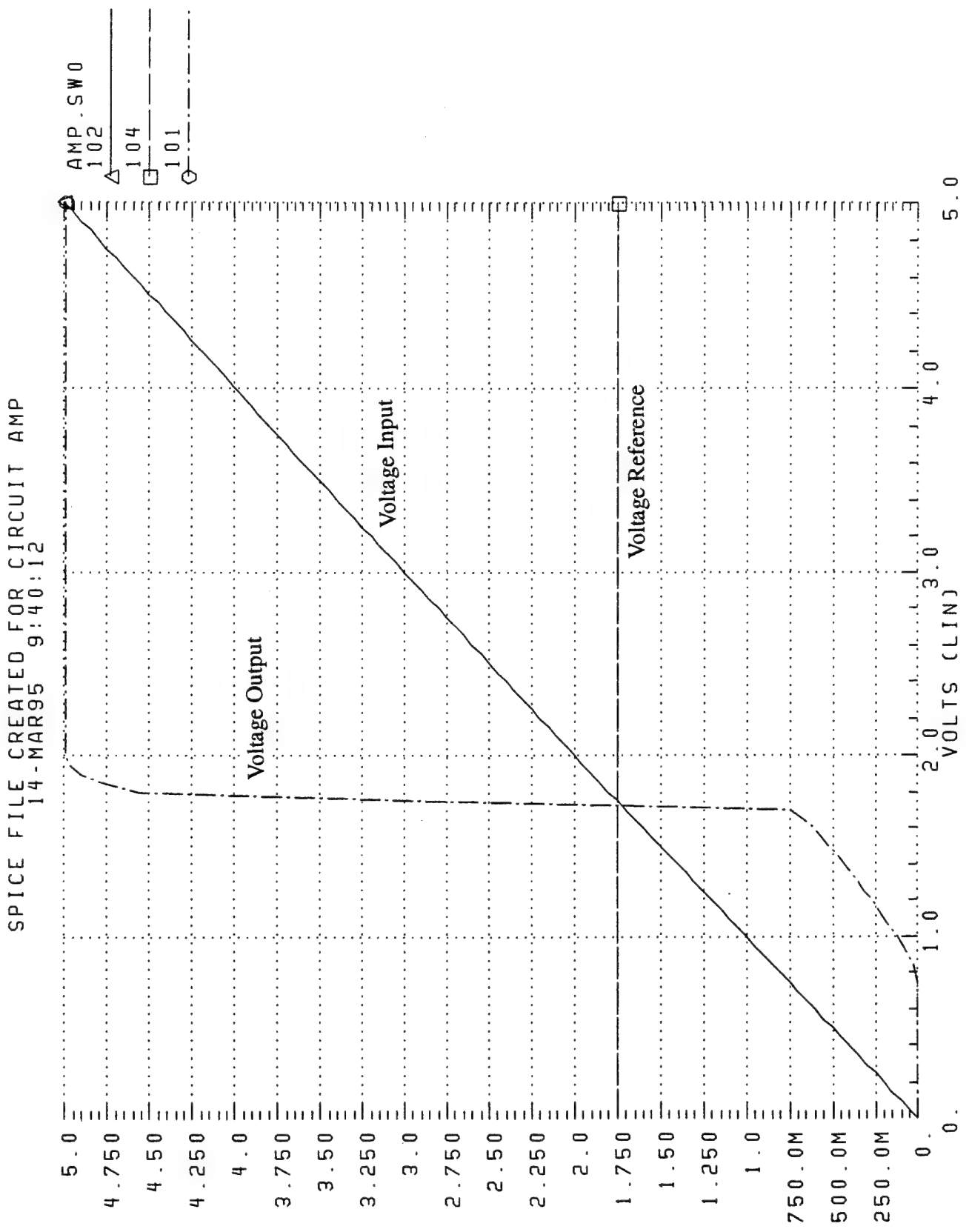

Figure 48. HSPICE Simulation Results for Differential Amplifier Circuit.

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